BASICS

<table>
<thead>
<tr>
<th>Voltage Gain:</th>
<th>( A_v = \frac{V_o}{V_i} )</th>
<th>( A_v(dB) = 20 \log[A_v] )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Gain:</td>
<td>( A_p = \frac{P_o}{P_i} = \frac{V_o I_o}{V_i I_i} = A_v A_I )</td>
<td>( A_p(dB) = 10 \log[A_p] )</td>
</tr>
<tr>
<td>Current Gain:</td>
<td>( A_i = \frac{i_o}{i_i} )</td>
<td>( A_i(dB) = 20 \log[A_i] )</td>
</tr>
</tbody>
</table>

When the gain \( A_v \) or \( A_i \) is negative it means there is a 180° phase shift between input and output. When a gain expressed in decibels is negative, it means the signal is attenuated.

Efficiency:

\[ \eta = \frac{P_L}{P_{dc}} \]

\[ P_{dc} + P_L = P_I + P_{dissipated} \]

If a circuit is linear, it means it can be described by linear equations (no exponents).

AC-DC NOTATION CONVENTIONS:

\[ V_B = V_b + V_B \]

\[ V_B = DC \text{ voltage [V]} \]

\[ V_b = AC \text{ (signal) voltage [V]} \]

UNITS CONVENTION

For this class, currents were in terms of mA and resistances were in term of kΩ.
THÉVENIN AND NORTON EQUIVALENTS

A one-port network (circuit presenting 2 external terminals) may be represented by either a Thévenin or Norton equivalent. Note that \( R_{\text{EQ}} \) has the same value in both the Thévenin and Norton equivalents.

### THÉVENIN EQUIVALENT

\[
\begin{align*}
V_{\text{TH}} &+ \\
R_{\text{EQ}} &- \\
\end{align*}
\]

The Thévenin voltage \( V_{\text{TH}} \) is the open-circuit voltage. The Norton current \( I_N \) is the short-circuit current.

It is only necessary to find one or the other. If there are no independent sources (dependent sources may be present) then \( V_{\text{TH}} = I_N = 0 \) and the circuit reduces to an equivalent resistance.

To find \( R_{\text{EQ}} \):
1) “Turn off” the independent sources, i.e. voltage sources go to zero which means they are shorted and current sources also go to zero which means they are opened.
2) If there are independent and dependent sources, turn off the independent sources and apply a test source (\( V_{\text{TEST}} = 1 \) or \( I_{\text{TEST}} = 1 \)) to the port. Calculate the unknown parameter \( V_{\text{TEST}} \) or \( I_{\text{TEST}} \) at the port and find \( R_{\text{EQ}} \) using

\[
R_{\text{EQ}} = \frac{V_{\text{TEST}}}{I_{\text{TEST}}}
\]

### NORTON EQUIVALENT

\[
\begin{align*}
I_N &+ \\
R_{\text{EQ}} &- \\
\end{align*}
\]

### THÉVENIN/NORTON EXAMPLE

Given this circuit:

\[
\begin{align*}
\begin{array}{c}
\text{4 } \Omega \\
\text{12 } \text{V} \\
\end{array} & \begin{array}{c}
\text{4 } \Omega \\
\end{array} & \begin{array}{c}
\text{4 } \Omega \\
\end{array} & \begin{array}{c}
R_L \\
\end{array}
\end{align*}
\]

The Thévenin voltage \( V_{\text{TH}} \) is the open-circuit voltage, i.e. with the load disconnected.

The Thévenin resistance is the equivalent resistance with the independent voltage source shorted and the load disconnected.

The Thévenin equivalent circuit can now be written as:

\[
\begin{align*}
V_{\text{TH}} & = I_N R_{\text{TH}} \\
\text{And the Norton equivalent can be written as:}
\end{align*}
\]

### 2-PORT LINEAR NETWORKS

All may be described by (4 variables: \( R_1, R_2, K, \alpha \)):

\[
\begin{align*}
\begin{array}{c}
R_1 \\
\end{array} & \begin{array}{c}
\alpha v_{\text{out}} \\
+ \\
K v_{\text{in}} \\
\end{array} & \begin{array}{c}
R_2 \\
\end{array} & \begin{array}{c}
v_{\text{out}} \\
+ \\
\end{array}
\end{align*}
\]

If \( \alpha \) is close to zero, we can use (3 variables: \( Z_{\text{in}}, Z_{\text{out}}, K \)):

\[
\begin{align*}
\begin{array}{c}
Z_{\text{in}} \\
\end{array} & \begin{array}{c}
v_{\text{in}} \\
+ \\
\end{array} & \begin{array}{c}
K v_{\text{in}} \\
\end{array} & \begin{array}{c}
Z_{\text{out}} \\
\end{array} & \begin{array}{c}
v_{\text{out}} \\
+ \\
\end{array}
\end{align*}
\]

### PARALLEL RESISTANCE

\[
R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2}
\]

\[
R_1 \parallel R_2 \parallel \cdots \parallel R_N = \frac{1}{R_1^{-1} + R_2^{-1} + \cdots + R_N^{-1}}
\]

### VOLTAGE DIVISION

\[
V_{\text{out}} = \frac{R_2}{R_1 + R_2} V_s
\]

### CURRENT DIVISION

\[
I_1 = \frac{R_2}{R_1 + R_2} I_s
\]

\[
I_2 = \frac{R_1}{R_1 + R_2} I_s
\]

### SHORTCUTS AND TRICKS:

The circuit is simplified by recognizing a Norton equivalent and converting to a Thévenin equivalent.
A resistance in parallel with a voltage source or in series with a current source may be eliminated.

**VOLTAGE SOURCE**

\[ V_S - V_{TH} = \frac{V_{TH}}{R} \]

**CURRENT SOURCE**

\[ I = I_{TH} \]

When a dependent current source and the current on which it depends both feed into a resistor as shown, the two components may be replaced by a single resistance \( R_{EQ} \) calculated as follows:

\[ R_{EQ} = (K + 1)R \]

If the direction of \( i \) was reversed then

\[ R_{EQ} = (K - 1)R \]

When a current source is dependent on the voltage across itself, it may be replaced by a resistor equal to the inverse of the current source’s coefficient:

\[ K = \frac{1}{R} \]

A dependent voltage source may be replaced with a resistor providing the same voltage drop in order to find \( V_{TH} \). However, this **cannot** be used to find \( R_{EQ} \).

A current source may be rerouted to another point provided a second source of equal magnitude is created with flow from that point to the original. \( I \) may be independent or dependent.
DIODES

FORWARD-BIASED DIODE

\[ \begin{align*}
  & i \\
  & + \quad v \\
  & \text{anode} \quad \text{cathode}
\end{align*} \]

CHARACTERISTICS OF THE IDEAL DIODE
• If \( v \) is negative, the diode is reversed biased and acts as a closed switch with \( v = 0 \).
• If a positive current is applied in the direction shown, the diode is forward biased and acts like an open circuit.

CHARACTERISTICS OF A REAL DIODE
• If \( v \) is negative, the diode is reversed biased. If the magnitude of \( v \) is small, the diode conducts little until the magnitude of \( v \) reaches the breakdown voltage at which point the diode conducts.
• If a positive current is applied in the direction shown, the diode is forward biased. There is not a significant amount of conduction until the voltage reaches about 0.7V.

THE I-V RELATIONSHIP IN THE FORWARD-BIAS REGION

\[ I_D = I_S (e^{V_D/nV_T} - 1) \]

The -1 is unimportant since the \( e^{V_D/nV_T} \) term is on the order of 10\(^{12}\) so it is eliminated:

\[ I_D = I_S e^{V_D/nV_T} \]

\[ \ln(I_D / I_S) = V_D / nV_T \]

SIGNAL ANALYSIS
The total signal is the AC signal plus the DC signal.
For AC signal analysis, turn off DC sources.
Consider the diode as a resistance \( r_d \).
For DC analysis, turn off AC sources.

\[ r_d = \frac{nV_T}{I_D} \]

THERMAL VOLTAGE

| \( V_T \) = thermal voltage, \( \approx 25 \text{ mV} \) |
| \( k \) = Boltzmann's constant, \( 1.38 \times 10^{-23} \text{ joules/kelvin} \) |
| \( T \) = absolute temperature (kelvins), 273 + temp. in °C |
| \( q \) = magnitude of electronic charge, \( 1.60 \times 10^{-19} \text{ coulomb} \) |

RECTIFIER CIRCUITS

2-DIODE FULL-WAVE RECTIFIER

\[ \begin{align*}
  & I_L \\
  & V_{sm} \\
  & C \\
  & R_L
\end{align*} \]

FULL-WAVE BRIDGE RECTIFIER

\[ \begin{align*}
  & I_L \\
  & V_{sm} \\
  & C \\
  & R_L
\end{align*} \]

Formulas apply for small ripple voltages:

\[ V_{ripple} = \frac{V_{sm}}{2fR_C} \]

\[ V_L = V_{sm} - \frac{V_{ripple}}{2} \]

\( V_{ripple} \) = ripple voltage, peak to peak
\( V_{sm} \) = transformer voltage, peak
\( f \) = frequency [Hz]
\( R_L \) = load resistance [Ω]
\( C \) = capacitance [F]
BIPOLAR JUNCTION TRANSISTORS - DC ANALYSIS

**Bias**: the difference in DC potential between base and emitter.

**DC ANALYSIS MODEL (NPN)**
For PNP, reverse the polarities of the diode and voltage supply. \( I_b \) and \( \beta I_b \) remain as shown but will have negative values.

**Q-POINT**:
The Q-Point (also quiescent point, dc bias point, or operating point) is the center of the transfer characteristic (operating voltage range). It is adjusted by setting the DC voltage level of the base terminal.

**Rule of Thumb**: To set the Q-Point, let

\[
V_B = R_C I_C = \frac{1}{3} V_{CC}
\]

and

\[
I_1 = 10 I_B = 10 - \frac{I_E}{\beta + 1}
\]

where \( I_1 \) is the current through the base-to-ground resistor.

A transistor amplifier is biased so that the Q-Point is located near the center of the DC Loadline. When an AC signal is applied, the Q-Point oscillates along the loadline.

**BASE CURRENT**:
The relationships among the emitter, base, and collector currents are functions of \( \beta \). The relationships apply to signal current as well as DC current.

\[
I_C = \beta I_B \quad I_E = (\beta + 1) I_B
\]

**\( \alpha \) AND \( \beta \)**:
\( \alpha = \frac{I_C}{I_E} \quad \beta = \frac{I_C}{I_B} \)

\( \alpha \) is constant for a particular transistor. It’s value is less than but close to 1, normally 0.98-0.9995. \( \alpha \) is the gain of a Common-Base amplifier.

\( \beta \) is constant for a particular transistor, typically in the range of 100 to 200 but may be 50-2000. Since the value of \( \beta \) may vary significantly among transistors of the same type, a \( \beta \)-tolerant circuit design is desirable. \( \beta \) is the Common-Emitter current gain.

**CURRENT MIRROR**
In this circuit, the base voltage is at -14.3V due to the 0.7V drop across the BE junctions. Since \( Q_1 \) is also at -14.3V, \( I_{C1} \) will be ½mA. If all transistors are identical, then their base currents will be equal and \( I_{C1} = I_{C2} = I_{C3} = \frac{1}{2} mA \). \( Q_2 \) and \( Q_3 \) can be used as current sources to bias other transistors.
BIPOLAR JUNCTION TRANSISTORS - AC ANALYSIS

CIRCUIT LOADING

**Loading** is the loss of signal due to circuit resistance. Some of the signal is lost in $R_s$; some output is lost in $Z_{out}$:

\[
\text{gain} = \frac{v_{out}}{v_{in}} = K \frac{Z_{in} \cdot R_L}{Z_{in} + R_s \cdot R_L + Z_{out}}
\]

**DETERMINING IMPEDANCE**

**TO FIND $Z_{in}$:**

1. Remove the input source.
2. Leave the load connected.
3. Short other independent voltage sources; open other independent current sources.
4. If there are no dependent sources, the input impedance is determined by inspection, otherwise continue to step 5.
5. Keep in mind that current could flow in the circuit. Either a) manipulate the circuit using resistance reflection rule to ground out the independent sources, b) apply a test source to the input, or c) use other Tricks (p.2) to redraw the circuit.

**TO FIND $Z_{out}$:**

1. Remove the load.
2. Turn off the input source, but leave the source (resistance) connected.
3. Short other independent voltage sources; open other independent current sources.
4. If there are no dependent sources, the output impedance is determined by inspection, otherwise continue to step 5.
5. Keep in mind that current could flow in the circuit. Either a) manipulate the circuit using resistance reflection rule to ground out the independent sources, b) apply a test source to the output, or c) use other Tricks (p.2) to redraw the circuit.

When calculating the gain, $v_{out}/v_{in}$, assume that sources and load (if shown) are connected.

**EQUATIONS FOR AC ANALYSIS**

<table>
<thead>
<tr>
<th>Equation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$g_m = 40I_C$</td>
<td>transconductance [mA/V]</td>
</tr>
<tr>
<td>$V_T = 25$ mV</td>
<td>thermal voltage</td>
</tr>
<tr>
<td>$I_C = \beta$</td>
<td>collector current from DC analysis</td>
</tr>
<tr>
<td>$V_A = \beta I_C$</td>
<td>a parameter of the particular BJT typically in the range of 50-100 volts, called the Early voltage</td>
</tr>
<tr>
<td>$r_e = \frac{1}{g_m} = \frac{1}{\beta + 1}$</td>
<td>base resistance</td>
</tr>
</tbody>
</table>

**HYBRID π Small Signal Model for BJT Transistor**

This works for PNP or NPN transistors without modification.

The same model is shown drawn 2 different ways. ($r_o$, which is shown with dashed lines in the model at left, may usually be ignored.)

**HYBRID T Small Signal Model for BJT Transistor**

This works for PNP or NPN transistors without modification.

The same model is shown drawn 2 different ways. The T model is used if we can neglect $r_o$, that is $r_o$ is very large.

**RESISTANCE REFLECTION RULE**

The HYBRID π and the HYBRID T models are again redrawn to illustrate conversion between the two:

One model is easily converted to the other. $r_\pi$ is related to $r_e$ by a factor of $(\beta + 1)$. This has the effect of shifting the resistance between the base and emitter legs as shown above. A way to remember whether to multiply or divide is to know that base current is smaller than emitter current, so the base resistance must be larger. This is a powerful tool in AC analysis because other series resistances in the circuit may be combined with $r_\pi$ or $r_e$ and shifted with them.
Differential amplifiers are used in integrated circuit design. In IC design, large capacitors and large (Ω) resistors are impractical. In this circuit, Q2 eliminates the need to have a bypass capacitor to ground by providing a low-resistance path to signal ground.

For AC analysis of differential amplifiers, we divide the input signals into differential and common-mode components. The inputs are written as

\[ v_{i1} = v_{icm} + \frac{v_{id}}{2} \]
\[ v_{i2} = v_{icm} - \frac{v_{id}}{2} \]

We solve for each separately using different models and then combine the results. For a description of the circuit analysis of the Single-Ended Output Differential Amplifier shown above, see the file DifferentialAmplifierSEO.pdf.

**DIFFERENTIAL VOLTAGE GAIN**

\[ A_d = \frac{v_{o d}}{v_{id}} \]

\[ v_{o d} = \text{total differential output voltage} \quad [\text{V}] \]

\[ v_{id} = \text{total differential input voltage} \quad [\text{V}] \]

**COMMON-MODE VOLTAGE GAIN**

\[ A_{cm} = \frac{v_{ocm}}{v_{icm}} \]

\[ v_{ocm} = \text{common-mode output voltage} \quad [\text{V}] \]

\[ v_{icm} = \text{common-mode input voltage} \quad [\text{V}] \]

**COMMON-MODE REJECTION RATIO (CMRR)**

\[ CMRR = \left| \frac{A_d}{A_{cm}} \right| \]

\[ CMRR_{dB} = 20 \log_{10} \left| \frac{A_d}{A_{cm}} \right| \]

**THE MILLER EFFECT**

The existence of \( C_\mu \) complicates the above model. The Miller effect says that the model can be approximated by removing \( C_\mu \) and replacing it with another gate-to-source capacitance \( C_M \). \( K \) is the voltage gain across \( C_\mu \) (assuming that \( C_\mu \) represents an open circuit).

**HIGH-FREQUENCY ANALYSIS**

Small capacitances exist between the base and collector and between the base and emitter. These affect the frequency characteristics of the circuit.

We solve for each separately using different models and then combine the results. For a description of the circuit analysis of the Single-Ended Output Differential Amplifier shown above, see the file DifferentialAmplifierSEO.pdf.
METAL OXIDE SILICON FIELD-EFFECT TRANSISTORS - MOSFETs

**Enhancement MOSFET**

n-channel type: When a positive voltage is applied to the gate of the n-channel MOSFET shown at right, a channel of n material is formed within the p region near the gate. This enables current flow from drain to source. The substrate or base is usually internally connected to the source, forming a 3-terminal device.

<table>
<thead>
<tr>
<th>n-channel (NMOS)</th>
<th>p-channel (PMOS)</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image" alt="Diagram" /></td>
<td><img src="image" alt="Diagram" /></td>
</tr>
</tbody>
</table>

**Depletion MOSFET**

The n-channel Depletion MOSFET, as shown in the diagram at right, has an n-channel built in that allows current flow from drain to source. When a negative voltage is applied to the gate terminal, the channel becomes p material so that current flow is stopped.

<table>
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<tr>
<th>n-channel (NMOS)</th>
<th>p-channel (PMOS)</th>
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<td><img src="image" alt="Diagram" /></td>
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</tr>
</tbody>
</table>

The Three Modes of Operation

**CUTOFF** - The region where the gate voltage is lower than the threshold voltage $V_t$, so that no current flows through the drain.

**TRIODE** - The region where $V_{DS}$ is lower than the excess gate voltage and the characteristic curve is a curve. For small signals, the FET behaves like a voltage-controlled resistor. In the operating region, the characteristic curve may be thought of as a straight line, the slope of which is the inverse of the drain-to-source resistance.

**SATURATION** - The region where $V_{DS}$ is greater than the excess gate voltage and the characteristic curve is a horizontal line. Drain current is a function of gate voltage $V_{GS}$. Drain current is constant (current saturated) with changes of $V_{DS}$.

**THRESHOLD VOLTAGE** - $V_t$, the gate-to-source voltage at which an FET begins to conduct, usually 1 to 3 volts in an n-channel enhancement MOSFET.

**EXCESS GATE VOLTAGE or EFFECTIVE VOLTAGE** - The gate-to-source voltage in excess of the threshold voltage, i.e. $V_{GS} - V_t$.

**ASPECT RATIO** - $W/L$ - the ratio of the channel width to the channel length (distance from source to drain).

**CMOS (complementary MOS)** - employing both n-channel (NMOS) and p-channel (PMOS) on the same chip.

**GATE CAPACITANCE** - The gate and substrate are separated by a thin, non-conducting metal oxide layer which causes the gate to act like a capacitor. It is necessary to connect a resistor between gate and ground to prevent a destructive charge from accumulating. The resistor should be on the order of 1 Meg to preserve the high impedance input characteristic.

**DC DRAIN CURRENT**

$$I_D = \frac{1}{2} k' \left( \frac{W}{L} \right) (v_{gs} - V_t)^2$$

This formula results in a quadratic equation with two answers. The lower value is the correct answer; or write an equation for $v_{gs}$ and plug in values to see which works, i.e. $v_{gs} = V_g - V_s$.

$$k' = \mu_n C_{ox}$$

$W$ is the channel width

$L$ is the channel length

$V_{gs}$ is the gate to source voltage

$V_t$ is the threshold voltage

$k'$ is the process transconductance parameter [$A/V^2$]

$\mu_n$ is the electron mobility in the channel. Typical value is 580 $cm^2/Vs$

$C_{ox}$ capacitance per unit area of the gate channel capacitance--permittivity of the silicon oxide divided by its thickness [$F/m^2$]
MOSFETs - AC ANALYSIS and FREQUENCY ANALYSIS

SMALL-SIGNAL MODELS
The circuit models for NMOS and PMOS FETs are the same. The arrow in the model’s current source always points toward the FET’s source terminal. This is the terminal of the circuit symbol which has an arrow, though the circuit symbol arrow may point either direction. The value of $g_m$ is small and the value of $r_o$ is large for FETs. This may affect what can be ignored.

\[ g_m = \sqrt{2k'(W/L)} I_D^{1/2} \]
\[ r_o = \frac{V_A}{I_D} \]

T-Model (seldom used)
Caution: Though it may not look like it, the input impedance is still infinity. No current flows through the gate.

SOURCE DEGENERATION
When a source resistance is present, it can be incorporated into the small-signal model, changing $g_m$, $v_{gs}$, and $r_o$. This is an approximation that assumes $g_m r_o >> 1$.

CASCODE AMPLIFIER
$r_0$ acts as a degeneration resistance for $Q_2$, giving very high output impedance. The low impedance looking into the source of $Q_2$ guarantees that virtually all of the transconductance current $g_m v_{gs}$ of $Q_1$ will find its way to the load. Good high-frequency input characteristics. High output impedance.

FREQUENCY ANALYSIS
Small capacitances exist between the gate and drain and between the gate and source. These affect the frequency characteristics of the circuit.

THE MILLER EFFECT
The existence of $C_{gd}$ complicates the above model. The Miller effect says that the model can be approximated by removing $C_{gd}$ and replacing it with another gate-to-source capacitance $C_M$. $K$ is the voltage gain across $C_{gd}$ (assuming that $C_{gd}$ represents an open circuit).

THE POLES OF AN AMPLIFIER
The poles of an amplifier are the frequencies at which the frequency response has dropped off by 3 dB, also called the corner frequencies. The CG model below has an input pole and an output pole.
### EQUATION SUMMARY

<table>
<thead>
<tr>
<th></th>
<th>BJT</th>
<th>MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DC Current</strong></td>
<td>$I_C = \beta I_B$</td>
<td>$I_D = \frac{1}{2} k'(\frac{W}{L})(V_{gs} - V_I)^2$</td>
</tr>
<tr>
<td><strong>Circuit Model Transconductance</strong></td>
<td>$g_m = 40I_C$</td>
<td>$g_m = \sqrt{2k'(W/L)I_D^{1/2}}$</td>
</tr>
<tr>
<td><strong>Circuit Model Resistances</strong></td>
<td>$r_n = \frac{\beta}{g_m}$</td>
<td>$r_o = \frac{V_A}{I_D}$</td>
</tr>
<tr>
<td></td>
<td>$r_o = \frac{V_A}{I_C}$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$r_c = \frac{r_n}{\beta + 1}$</td>
<td></td>
</tr>
<tr>
<td><strong>Differential Amplifier</strong></td>
<td>$A_d = \frac{v_{od}}{v_{id}}$</td>
<td>$A_{cm} = \frac{v_{ocm}}{v_{icm}}$</td>
</tr>
<tr>
<td>Gain and Common-mode Rejection Ratio</td>
<td>CMRR = $\frac{</td>
<td>A_d</td>
</tr>
<tr>
<td><strong>Source Degeneration Model</strong></td>
<td>$g'_m = \frac{g_m}{1 + g_m R_S}$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$r'_o = (1 + g_m R_S) r_o$</td>
<td></td>
</tr>
<tr>
<td><strong>Cascode Amplifier Model</strong></td>
<td>$g'_m = g_m R'_D = R_D$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$r'_o = r_o (1 + g_m r_o)$</td>
<td></td>
</tr>
<tr>
<td><strong>Miller Effect</strong></td>
<td>$K = \frac{v_C}{v_x}$</td>
<td>$K = \frac{v_D}{v_G}$</td>
</tr>
<tr>
<td></td>
<td>$C_M = (1 - K)C_\mu$</td>
<td>$C_M = (1 - K)C_{gd}$</td>
</tr>
<tr>
<td><strong>Amplifier Poles or Corner Frequency</strong></td>
<td>$\omega = \frac{1}{\tau} = \frac{1}{RC}$</td>
<td></td>
</tr>
</tbody>
</table>
# TYPES OF SINGLE-TRANSISTOR AMPLIFIERS

<table>
<thead>
<tr>
<th>Common Collector or Emitter Follower (BJT)</th>
<th>Common Drain or Source Follower (MOSFET)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage gain is dependent on $\beta$. By adding a resistance at the emitter terminal, this dependence is reduced, input resistance is increased, voltage gain is reduced, and high-frequency response is improved.</td>
<td></td>
</tr>
<tr>
<td>Common Source (MOSFET)</td>
<td>Voltage gain is less than one</td>
</tr>
</tbody>
</table>

- Current gain
- Power gain
- Low output impedance
- Voltage gain is less than one
- No Miller effect
- Used as a buffer amplifier or output stage

## BJT

<table>
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- Current gain
- Power gain
- Low output impedance
- Voltage gain is less than one
- No Miller effect
- Used as a buffer amplifier or output stage

## MOSFET

<table>
<thead>
<tr>
<th>Common Collector or Emitter Follower (BJT)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage gain is dependent on $\beta$. By adding a resistance at the emitter terminal, this dependence is reduced, input resistance is increased, voltage gain is reduced, and high-frequency response is improved.</td>
</tr>
<tr>
<td>Common Source (MOSFET)</td>
</tr>
</tbody>
</table>

- Current gain
- Power gain
- Low output impedance
- Voltage gain is less than one
- No Miller effect
- Used as a buffer amplifier or output stage