2.8 SWITCHING VOLTAGE REGULATORS

The voltage regulators discussed thus far have been of the "dissipative" type. In these regulators the flow of current to the load is controlled by a series-pass circuit which produces a voltage drop equal to the required input–output voltage difference, $V_{IN} - V_O$. The input voltage is the unregulated d-c voltage. In performing this function the series-pass circuit must dissipate an amount of power equal to the difference between the input power $V_{IN}I_O$ and the output power V_OI_O. As a result, the efficiency of this type of voltage regulator will be quite low, being given by

$$\text{efficiency} = \eta = \frac{P_O}{P_{IN}} = \frac{V_OI_O}{V_{IN}I_O} = \frac{V_O}{V_{IN}} \tag{2.75}$$

The fraction of the input power that is dissipated in the voltage regulator will therefore be

$$\frac{P_{IN} - P_O}{P_{IN}} = {}_1 - \eta = \frac{V_{IN} - V_O}{V_{IN}} \tag{2.76}$$

Since the output voltage is typically in the range $0.5V_{IN}$ to $0.7V_{IN}$, we see that the circuit efficiency will typically be in the range 50 to 70%. As a result, some 30 to 50% of the input power will have to be dissipated by the regulator.

The power dissipation in the regulator is not a serious problem for regulators supplying less than about 1 W. However, for output power levels much in excess of this, and in particular for levels above 10 W, the circuit inefficiency and in particular the power that must be dissipated by the series-pass circuit may pose serious problems. Due to the power transistor and the associated heat sinking requirements, the regulator cost, size, and weight will escalate rapidly with increasing output power requirements.

A useful alternative to the dissipative type of voltage regulator is one of the switching type. In the dissipative regulator the series-pass transistors operate continuously in the active region wherein the combination of a substantial current flow and concurrently a major voltage drop results in a large power dissipation as given by $P_d = (V_{IN} - V_O)I_O$. In contrast to this, in the switching regulator the series-pass transistors are not operated in the active mode, but rather are switched back and forth between cutoff and saturation.

In the switching regulator the power flow to the load is controlled by the duty cycle of the series-pass transistors, that is, the fraction of time that these transistors are in the "on" state. A fraction of the output voltage is supplied to the control circuitry and therein compared to the reference voltage. The difference between the feedback voltage and the reference voltage is amplified and used to control the duty cycle of the series-pass transistors. If the output voltage is too low, the control circuitry

acts to lengthen the duty cycle, thus causing the output voltage to increase. If the output voltage is too high, the duty cycle is diminished and the output voltage decreases. In either case the output voltage will be stabilized at a level determined by the resistance ratio of the feedback voltage divider and the reference voltage. In Figure 2.25 a basic block diagram of a switching regulator is presented.

The power dissipation of the switching transistor will be relatively low. When the transistor is of the cutoff region of operation the current through the transistor will be negligibly small, so that the power dissipation will similarly be negligible. When the transistor is turned on, it will rapidly be driven into saturation by the control circuitry. In the saturation mode the voltage drop across the transistor will be relatively small, generally less than 1 V, and often down in the range of about 0.2 V. As a result of the small voltage drop across the transistor the instantaneous power dissipation will be correspondingly small. The only time in which there is a substantial amount of power dissipated in the transistor will be during the switching transition, when the transistor is passing through the active region in going from cutoff to saturation, or vice versa. The switching transition time will, however, represent only a very small fraction of the total time, so that the average power dissipation will be small. In Figure 2.26 the instantaneous power dissipation of the transistor as a function of time is presented.

If we now look at Figure 2.25, we see that a fraction $R_2/(R_1 + R_2)$ of the output voltage is fed back to the inverting input of the error amplifier, where it is compared to the reference voltage which is applied to the noninverting input of the error amplifier. The difference between the reference voltage and the feedback voltage is thus amplified and thence applied to the inverting input of the comparator.

The oscillator generates a triangular waveform at a fixed repetition frequency, and this voltage is applied to the noninverting input of the comparator. The output of the comparator will thus be in the high state during the time when the triangular voltage waveform is above the level of the error amplifier output, and it is during

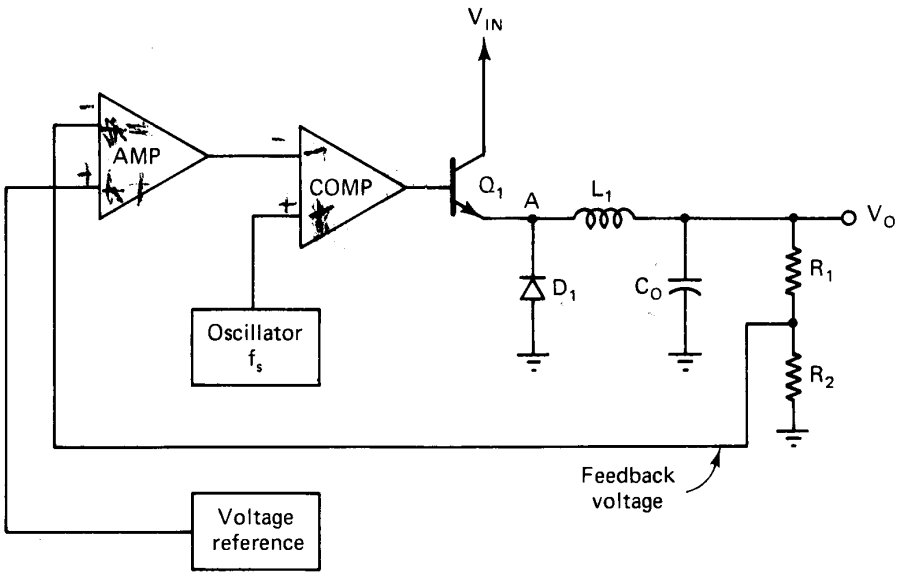

Figure 2.25 Basic diagram of a switching voltage regulator.

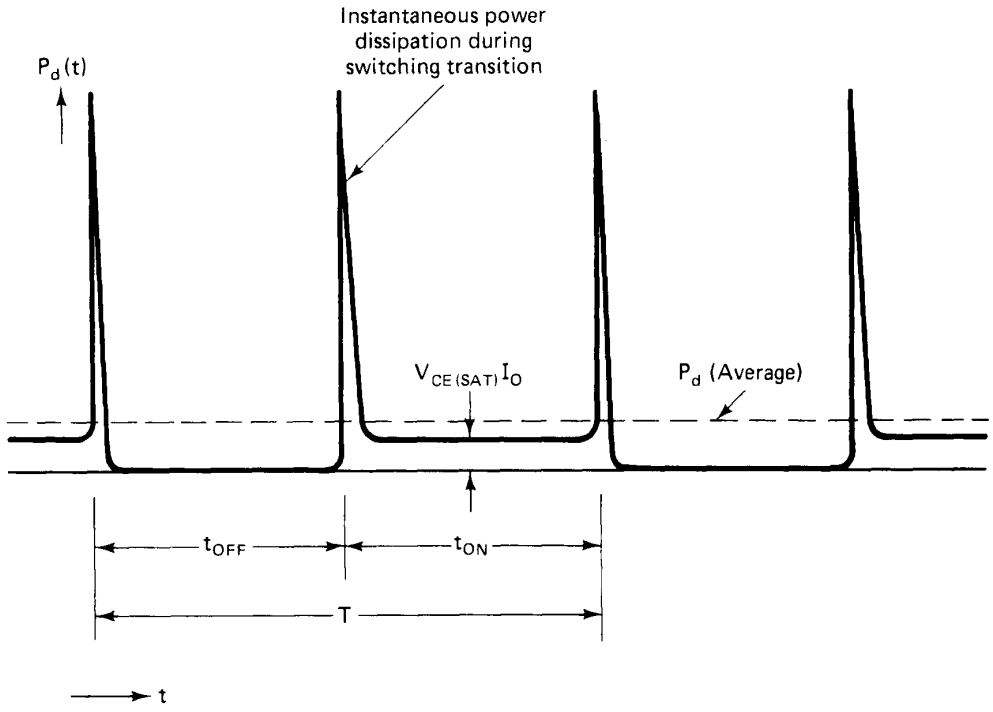

Figure 2.26 Instantaneous power dissipation of a switching transistor.

this time that the series-pass switching transistor will be turned on. During the remainder of the period the comparator output will be low and transistor Q_1 will be switched off. The output of the comparator is thus a pulse waveform, the period of which T is the same as the period of the oscillator output. The duty cycle, $\delta = t_{on}/T$, of the pulse waveform will be controlled by the difference between the feedback voltage and the reference voltage.

When Q_1 is on, the voltage applied to the inductor L_1 (at point A) will be $V_A = V \quad - V_{CE(SAT)} = V_{IN}$. This voltage will act to promote the flow of current through L_1. When Q_1 is turned off, the inductor L_1 will act to continue the current through itself and thus on to the load. Diode D_1 is used to provide a complete circuit during this period of time. When Q_1 is on, this diode will be biased off. Capacitor C_O acts to smooth out the voltage so that the output voltage will be a relatively smooth d-c voltage with very little a-c ripple.

During the time that Q_1 is off, the voltage at point A will be close to zero, actually one diode drop (0.7 V) below ground. The average voltage at point A will therefore be given by

$$\begin{aligned} V_A(\text{d-c}) &= (V_{IN} - V_{CE(SAT)})\frac{t_{on}}{T} + (-V_{D_1})\frac{t_{off}}{T} \\ &= V_{IN}\delta - V_{CE(SAT)}\delta - V_{D_1}(1-\delta) \\ &\simeq V_{IN}\delta \end{aligned} \tag{2.77}$$

Since L_1 and C_O will not affect the d-c voltage, the d-c voltage at the output will be the same as at point A, namely $V_O = V_A = V_{IN}$. Thus we see that the d-c output

voltage can be controlled or regulated by the control of the duty cycle by the feedback loop. The output voltage will be slightly smaller than V_{IN} due to $V_{CE(sat)}$ and the voltage drop of D_1. Both voltage drops will generally be in the neighborhood of about 0.7 V, so that we see that V_O will typically be around 0.7 V less than $V_{IN}(\delta)$. There will also be a small d-c voltage drop due to the series resistance of L_1, although this probably will not be in excess of about 0.1 V.

We have seen that the output voltage is controlled by the duty cycle $\delta = t_{on}/T$. For example, if $V_{IN} = 15$ V and V_O is to be 10 V, the duty cycle will be approximately given by $\delta = V_O/V_{IN} = 0.67$. Due to the transistor saturation voltage and the diode drop the duty cycle under steady-state conditions will actually have to be somewhat larger than this, probably around 0.70, so that Q_1 will be on for about 70% of the time (in saturation) and off (cutoff) for the remaining 30% of the time.

If the output voltage for some reason falls below 10 V, the feedback loop will act to increase the duty cycle and thereby bring the output voltage up to 10 V. Conversely, if for some reason, such as variations in load conditions or in line voltage, the output voltage goes above 10 V, the feedback loop will act to decrease the duty cycle and thereby bring the output voltage back down. The net result of the action of the feedback loop will be to regulate V_O at the design value given by $V_O = V_{REF}(1 + R_1/R_2)$. The entire system acts basically as a pulse width modulator (PWM) to control the duty cycle with which the series-pass switching transistor is driven.

The optimum switching frequency f_s is generally in the range 10 to 100 kHz. A high switching frequency will allow for relatively small values of L_1 and C_O to be used, thus reducing the size, weight, and cost of the system. On the other hand, as the switching frequency goes up, the power dissipated by the switching transistor will increase as a result of the increase in the number of switching transitions per unit time. This increase in the transistor power dissipation is the result of the finite switching speed of the transistor. To maximize the circuit efficiency, therefore, a power transistor with a fast switching speed should be chosen. As a result of these considerations a switching frequency in the range 10 to 100 kHz is usually chosen, often about 20 to 50 kHz.

2.8.1 Current Waveforms

Now that we have been introduced to the basic principles of operation of the switching regulator, we will consider the current waveform through L_1 and the a-c voltage ripple across C_O, and then conclude with a design example.

The inductance value of L_1 is chosen such that there will be a continuity of current flow through the inductor throughout the entire switching cycle. Indeed, both L_1 and C_O will be large enough such that the current waveform of the inductor current I_L will have an approximately triangular waveform superimposed on a d-c current level, which is equal to the load current. This is shown in Figure 2.27.

The relationship between the voltage across L_1 and the current through L_1 is given by $V_L = L(di_L/dt)$. As a result of the approximately linear slope of the current waveform, we can express this relationship during the "on" time as

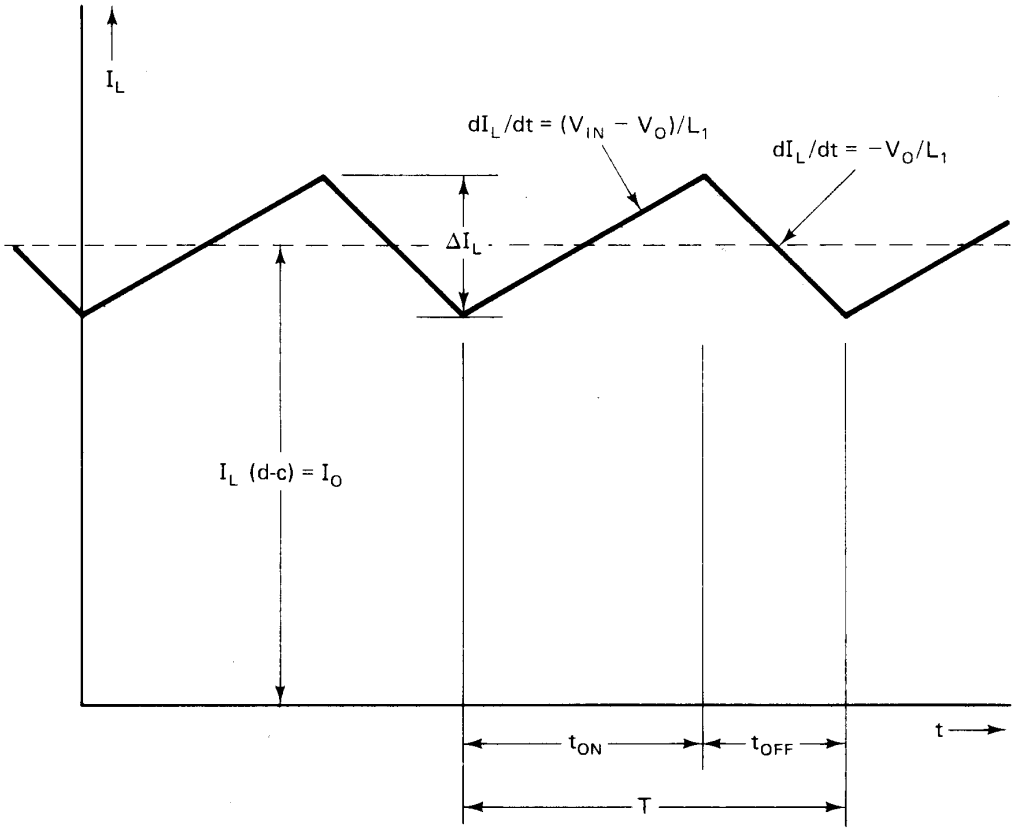

Figure 2.27 Inductor current waveform.

$$V_L = V_{IN} - V_O = L\frac{\Delta I_L}{t_{on}}$$

so that the change in the current during the "on" time will be given by

$$\Delta I_L = \frac{1}{L}(V_{IN} - V_O)t_{on} \tag{2.78}$$

During the "off" time the voltage across L_1 will be $-V_D - V_O = -V_O$, so that the change in the current through L_1 during this time period will be given by

$$\Delta I_L = \frac{1}{L}(-V_O)t_{off} \tag{2.79}$$

Since the current will be a continuous function of time, the algebraic sum of these two changes in the current must be zero, so that we have $(V_{IN} - V_O)t_{on} = V_O t_{off}$, giving $V_{IN}t_{on} = V_O(t_{on} + t_{off}) = V_O T$, and thus $V_O/V_{IN} = t_{on}/T = \delta$, which is the same as the result obtained earlier. A somewhat more rigorous analysis in which the transistor saturation voltage and the diode drop are taken into account will yield

$$V_O = V_{IN}\delta = V_{CE(SAT)}\delta - V_{D1}(1 - \delta) \tag{2.80}$$

which is again consistent with the previous results.

For the proper operation of this switching regulator, in particular for a maximally

smooth output waveform, it is important that the current through the inductor never never drop to zero or even reverse direction. Therefore, we must ensure that ΔI_L never approach the d-c inductor current level, which is the same as the d-c output current I_O. To take into account variations in I_O with loading conditions, a suitable safety factor will be to have $\Delta I_L \lesssim 0.4 I_O$. Since we can express ΔI_L as $\Delta I_L = (1/L) V_{ON} t_{off}$, we can solve for L_1 as

$$L_1 = \frac{V_O t_{off}}{\Delta I_L} \gtrsim \frac{V_O t_{off}}{0.4 I_O} \tag{2.81}$$

Since $t_{off} = T(1 - \delta)$, this can be rewritten as

$$L_1 \geq \frac{(V_O/I_O)T(1-\delta)}{0.4} = R_L T(1-\delta)2.5$$

2.8.2 Output Ripple Factor

The voltage at point A will be basically a repetitive pulse waveform with a duty cycle δ and an amplitude of approximately V_{IN}. The pulse waveform is applied to L_1 and C_O, which act as a low-pass filter to smooth out this voltage waveform and produce a d-c voltage across C_O that is the average value of the input voltage, V_{IN}.

The capacitance value for C_O will be such that the reactance of C_O at the a-c frequencies of interest will be small compared to the load resistance R_L. As a result, L_1 and C_O can, to a good degree of approximation, be considered at the a-c frequencies of interest to be a simple voltage divider. The ratio of the a-c output voltage at frequency f to the a-c input voltage at the same frequency will be given by

$$\frac{v_o(f)}{v_A(f)} = \frac{(1/j\omega C_O)}{j\omega L_1 + 1/j\omega C_O} \simeq -\frac{1}{\omega^2 L_1 C_O} \tag{2.82}$$

where $\omega = 2\pi f$ is the radian frequency. The negative sign for the voltage ratio is simply indicative of a 180° phase shift in the low-pass network.

To obtain an expression for the output a-c ripple voltage, we will consider the simple representative case of a 50% duty cycle for which case the d-c output voltage will be $V_O \simeq \frac{1}{2} V_{IN}$, and the voltage applied to the low-pass filter (at point A) will be a square wave of amplitude V_{IN} and period $T = 1/f_s$, where f_s is the oscillator frequency.

The Fourier series for this square wave will be given by

$$v_A(t) = V_{IN}\left(\frac{1}{2} + \frac{2}{\pi}\cos \omega t - \frac{2}{3\pi}\cos 3\omega t + \frac{2}{5\pi}\cos 5\omega t - \cdots\right) \tag{2.83}$$

where $\omega = 2\pi f_s$. We see that the input voltage to the low-pass filter will consist of a d-c component $V_{IN}/2$, a fundamental component at $f = f_s$, and various odd harmonic components at $f = nf_s$, where n is an odd integer. We further note that the amplitude of the various harmonic terms decreases as $1/n$.

The attenuation of the low-pass filter is proportional to f^2. This, together with the fact that the amplitudes of the various harmonic terms at the filter input decrease

as $1/n$, will mean that the dominant component of the output a-c ripple voltage with be the fundamental term at $f = f_s$, with the other harmonics being of relatively little importance.

The a-c output ripple voltage will therefore be given approximately by

$$v_o(\text{a-c}) = v_o(f_s) = \frac{2}{\pi} V_{IN} \frac{1}{\omega_s^2 L_1 C_O} \tag{2.84}$$

Since $V_O \simeq V_{IN}/2$ and $\omega_s = 2\pi f_s$, this can be rewritten as

$$v_o(\text{a-c}) = \frac{4}{\pi} V_O \frac{1}{4\pi^2 f_s^2 L_1 C_o} \simeq \frac{1}{30 f_s^2 L_1 C_o} V_O \tag{2.85}$$

The output ripple factor is the ratio of the peak-to-peak ripple voltage to the d-c output voltage. From the preceding equation we can thus directly write the ripple factor as

$$r = \text{ripple factor} = \frac{v_o(\text{a-c})_{\text{peak-to-peak}}}{V_O} \simeq \frac{1}{15 f_s^2 L_1 C_o} \tag{2.86}$$

We thus see that the ripple factor will be inversely proportional to the square of the switching frequency and to the $L_1 C_O$ product. With a high switching frequency, therefore, a moderately small value of inductance and capacitance can be used.

2.8.3 Design Example

For a design example we will stipulate the following:

I_O = d-c output (load) current = 1.0 A
V_O = d-c output voltage = 10 V
V_{IN} = 20 V
f_s = switching frequency = 30 kHz
output ripple factor = 0.05%

For the inductor L_1 we have the following requirement:

$$L_1 = \frac{R_L T(1-\delta)}{0.4} = \frac{2.5 R_L (1-\delta)}{f_s} = \frac{2.5 \times 10\ \Omega \times 0.5}{30\ \text{kHz}} \tag{2.87}$$

so that $L_1 = 417\ \mu\text{H}$. A choice of 500 μH will therefore be adequate. From the ripple factor condition we have

$$5 \times 10^{-4} \geq \frac{1}{15 f_s^2 L_1 C_o} = \frac{1}{15(30\ \text{kHz})^2 (500 \times 10^{-6}) C_O} \tag{2.88}$$

so that

$$C_O \geq 296\ \mu\text{F} \tag{2.89}$$

Therefore, a choice of 300 to 500 μF for C_O should prove satisfactory. The 0.05% ripple factor will correspond to a peak-to-peak output ripple voltage of only 5 mV, so that the d-c output waveform of this regulator circuit will be quite smooth.

2.8.4 Step-up Switching Voltage Regulator

The basic circuit of the switching regulator that has been discussed thus far is shown in Figure 2.28a. This type of switching regulator is called a step-down regulator since the output voltage is less than the input voltage (i.e., $V_O < V_{IN}$), and V_O is related to V_{IN} approximately by $V_O = \delta V_{IN}$, where $\delta = t_{on}/T$ is the duty cycle.

With the switching regulator it is also possible to achieve a voltage step up so that V_O will be greater than V_{IN}. The basic circuit of the step-up regulator is shown in Figure 2.28b.

It might at first be thought that it is not possible to have the output voltage greater than the input voltage. It is, however, the voltage induced in the inductor adding to the input voltage that produces an output voltage that is greater than the input voltage. During the time that Q_1 is off the reduction in the current through the inductor produces a voltage across the inductor given by $V_L = L(di_L/dt)$ that adds to V_{IN} to make V_O greater than V_{IN}. It should also be noted that even though $V_O > V_{IN}$, the output power $P_O = V_O I_O$ will not, of course, be any greater than the input power, $P_{IN} = I_{IN} V_{IN}$, since the input current will be larger than the output current.

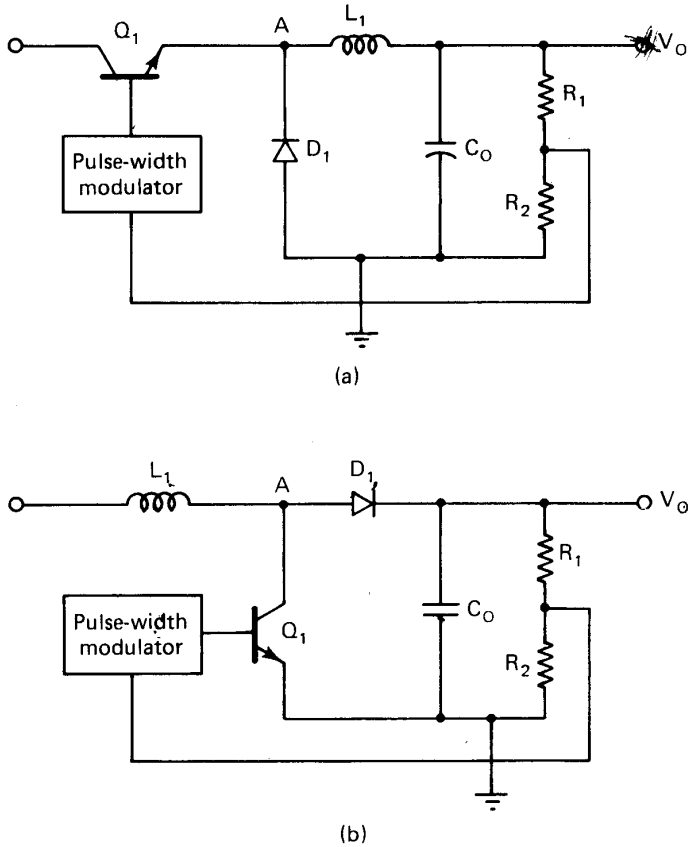

Figure 2.28 (a) Basic circuit of the step-down switching regulator; (b) basic circuit of the step-up switching regulator.

We can now easily derive the relationship between the input and output voltages of the step-up switching regulator. For this derivation we will assume that L_1 is large enough such that the current through L_1 will have a triangular waveform. During the time that Q_1 is off, the voltage across the inductor will be given by $V_{IN} - V_D - V_O = L(di_L/dt)$, where V_D is the forward-bias voltage drop of D_1 (about 0.7 V). Assuming a linear variation of current with time, we will therefore have that

$$\Delta I_L = \frac{1}{L}(V_{IN} - V_D - V_O)t_{off} \tag{2.90}$$

During the time interval that Q_1 is on (in saturation) we have that

$$V_{IN} - V_{CE(SAT)} = L\frac{di_L}{dt} \tag{2.91}$$

so that

$$\Delta I_L = \frac{1}{L}(V_{IN} - V_{CE(SAT)})t_{on}$$

Since the current flow through L_1 must be a continuous function of time, the algebraic sum of these two current changes must be zero, so that we have $\Delta I_L(t_{off}) + \Delta I_L(t_{on}) = 0$. Substituting in the equations above gives us

$$(V_{IN} - V_D - V_O)t_{off} + (V_{IN} - V_{CE(SAT)})t_{on} = 0 \tag{2.92}$$

Solving this for V_O gives

$$V_O = \frac{V_{IN}(t_{on} + t_{off}) - V_D t_{off} - V_{CE(SAT)}t_{on}}{t_{off}} \tag{2.93}$$

so that

$$V_O = V_{IN}\left(1 + \frac{t_{on}}{t_{off}}\right) - V_{CE(SAT)}(t_{on}/t_{off}) - V_D \tag{2.94}$$

Since V_D is approximately 0.7 V and $V_{CE(SAT)}$ will be less than 1 V, we see that it is quite possible to have V_O greater than V_{IN} if t_{off} is less than t_{on}. In terms of the duty cycle δ, the equation above can be rewritten as

$$V_O = \frac{V_{IN}}{1-\delta} - V_{CE(SAT)}\frac{\delta}{1-\delta} - V_D \tag{2.95}$$

For example, if we have that V_D and $V_{CE(SAT)}$ are both approximately 0.7 V, for a duty cycle of 0.7 and an input voltage of 10 V, we have

$$V_O = \frac{10}{0.3} - 0.7\left(\frac{0.7}{0.3}\right) - 0.7 \tag{2.96}$$

$$= 31 \text{ V}$$

Due to losses in L_1 and in the transistor during the switching transitions, the actual output voltage may be closer to 30 V. In any case, we see that a 3:1 voltage step-up has been achieved.

When Q_1 is on the voltage at point A will be $V_{CE(SAT)}$. When Q_1 is off, the voltage at point A will be equal to the input voltage plus the voltage induced in L_1 due to the falling current. This induced voltage will be approximately $V_{IN}(t_{on}/t_{off})$, so that the total voltage at point A during this time interval will be approximately $V_{IN}(1 + t_{on}/t_{off})$. This relationship can be readily obtained by noting that when Q_1 is on, the increase in the current through L_1 will be given by $\Delta I_L = (1/L)V_{IN}t_{on}$. When Q_1 is off, the change in the current will be $\Delta I_L + (1/L)(V_{IN} - V_A)t_{off}$. The diode drop and the transistor saturation voltage have been neglected for purposes of simplicity. Since the net change in the inductor current over the complete switching cycle must be zero, we have that $V_{IN}t_{on} + (V_{IN} - V_A)t_{off} = 0$, so that solving for V_A we have $V_A = V_{IN}(1 + t_{on}/t_{off})$.

In Figure 2.29 a diagram of the voltage waveform at point A is presented. Notice that this is a repetitive pulse waveform. The circuit to the right of point A, particularly the combination of the diode D_1 and the capacitor C_O, can be considered to be essentially a peak detector circuit giving an output waveform shown in Figure 2.29. During the pulses the capacitor will charge up via D_1 to the peak pulse amplitude $V_{IN}(1 + t_{on}/t_{off})$. Between pulses, however, the diode D_1 will be off so that the capacitor will discharge through the load. The rate of discharge of the capacitor will be $dQ_c/dt = I_O = V_O/R_L$, where R_L is the load resistance. If the circuit is designed for a low-output ripple factor V_O and therefore I_O will not change much on a percentage basis during the discharge time, the total charge lost by the capacitor during this time will be given by $\Delta Q_C = I_O t_{on} = V_O t_{on}/R_L$.

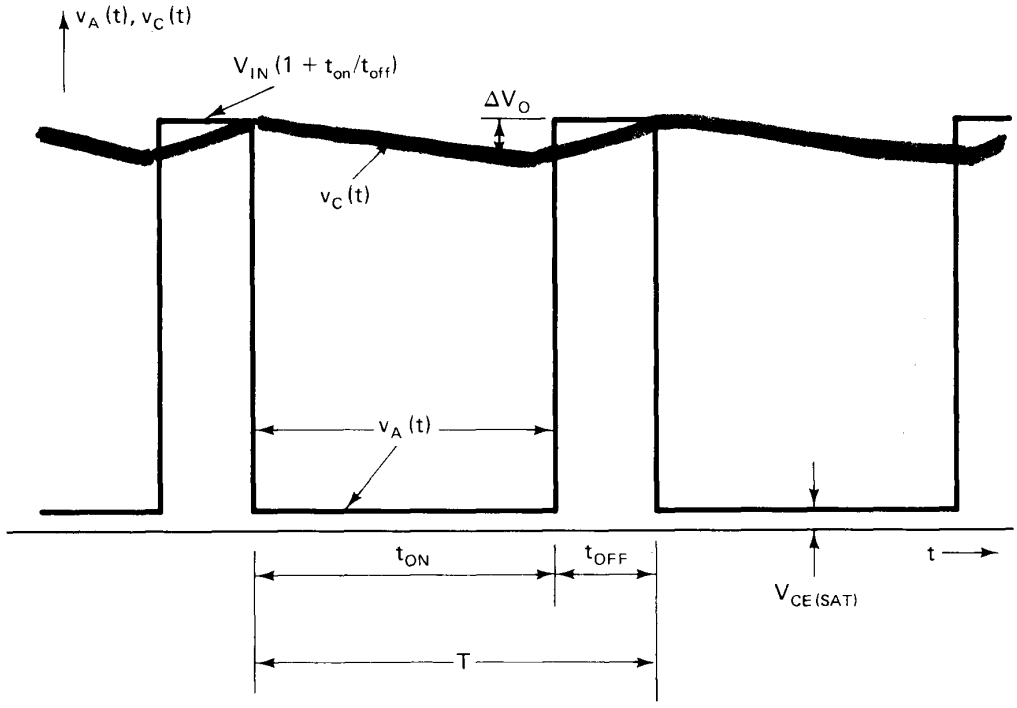

Figure 2.29 Voltage waveforms for step-up switching regulator.

The droop or sag in the output voltage at the end of the discharge time will be given by

$$\Delta V_O = \frac{\Delta Q_C}{C_O} = \frac{I_O t_{on}}{C_O} = \frac{V_O t_{on}}{R_L C_O} \tag{2.97}$$

This drop in the output voltage will be the peak-to-peak ripple voltage. The ripple factor will therefore be given by

$$\text{ripple factor} = R = \frac{\Delta V_O}{V_O} = \frac{t_{on}}{R_L C_O} = \frac{\delta T}{R_L C_O} = \frac{\delta}{f R_L C_O}$$

where f is the switching frequency.

For a representative example let us take $\delta = 0.7$, $f = 30$ kHz, $V_O = 30$ V, and $I_O = 0.5$ A. For a ripple factor at the output not to exceed 0.1%, the required value for C_O will be given by

$$C_O = \frac{\delta}{f R_L C_O} = \frac{0.7}{(30\text{ kHz} \times 60\ \Omega \times 0.001} \tag{2.98}$$
$$= 389\ \mu\text{F}$$

Thus a choice of a 500-μF, 50-V capacitor would prove to be satisfactory.

2.8.5 Effective Series Resistance

It is appropriate at this point to discuss another important factor in the capacitor selection for switching voltage regulators. This factor is the "effective series resistance" or ESR of the capacitor. Any real capacitor will exhibit together with the desired capacitance effect a parasitic series resistance, R_S, which is the effective series resistance. This series resistance will vary somewhat with frequency and with temperature.

To illustrate the importance of the ESR in the capacitor specification we will return to a consideration of the preceding example. During the discharge interval the current flowing out of the capacitor will be I_O, so that the additional drop in the capacitor voltage due to R_S will be $I_O R_S$. During the charge interval (D_1 on, Q_1 off) the charge supplied to the capacitor must make up for the charge lost during the discharge time, so that we will have

$$I_C t_{off} = I_O t_{on}$$

and thus

$$I_C = I_O \frac{t_{on}}{t_{off}} \tag{2.99}$$

where I_C is the current into the capacitor during the charging time. During this time interval there will be an additional rise in the capacitor voltage due to R_S given by $\Delta V_C = \Delta V_O = I_O R_S (t_{on}/t_{off})$. Therefore the increase in the peak-to-peak ripple voltage due to the effects of R_S will be given by

$$\Delta V_{O(\text{peak-to-peak})} = I_O R_S \left(1 + \frac{t_{on}}{t_{off}}\right) = I_O R_S \frac{V_O}{V_{IN}} \tag{2.100}$$

For a 0.1% ripple factor and a 10-V output voltage, the corresponding peak-to-peak ripple voltage will be 10 mV. For an output current of 0.5 A and a step-up voltage ratio of 3 : 1, the maximum allowable value of R_S will be given by the condition that

$$10\text{ mV} = 0.5\text{ A} \times R_S \times 3 \tag{2.101}$$

so that

$$R_S = \frac{10\text{ mV}}{1.5\text{ A}} = 7\text{ m}\Omega$$

This low value of effective series resistance may be very difficult to achieve in practice so that the 0.1% ripple factor may not be readily achievable. We see therefore that the ESR may be the dominant factor in determining the ripple factor and is therefore a very important factor in the capacitor selection.

2.8.6 Self-Oscillating Switching Regulators

The switching regulators described thus far have been of the externally excited or driven type, in which an oscillator or square-wave generator external to the voltage regulator circuit is used to determine the switching frequency. The regulator circuit itself acts as a pulse-width modulator to control the duty cycle of the pulses supplied by the oscillator.

In the interest of greater overall circuit simplicity it is possible to have a self-oscillating switching regulator in which a separate oscillator circuit is not needed. The self-excited condition of the switching regulator arises by means of a positive-feedback loop, as shown in Figure 2.30.

The positive feedback is obtained via the R_3–R_4 voltage divider. A small fraction

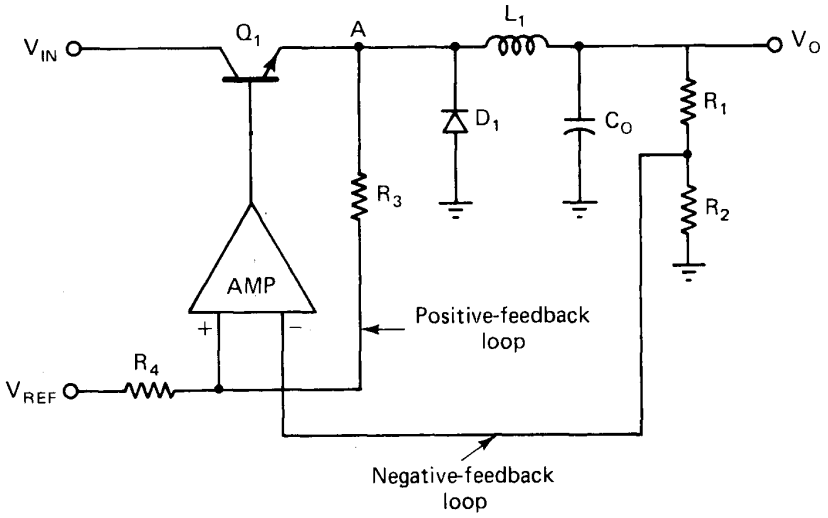

Figure 2.30 Basic diagram of the self-oscillating switching regulator.

of the voltage (typically 0.01 to 0.001) of the voltage at point A is fed back to the noninverting input of the error amplifier together with the reference voltage. There is at the same time negative feedback via the R_1–R_2 voltage divider in which a fraction of the output voltage is fed back to the inverting input of the amplifier.

To see how the self-oscillating switch regulator operates, let us start off when the input voltage is first applied, so that V_O starts off at zero. The reference voltage applied to the amplifier will cause Q_1 to turn on and go into saturation and V_O will start to increase. This will continue until the output voltage reaches a value such that the voltage fed back to the inverting input via the R_1–R_2 voltage divider equals the voltage applied to the noninverting input. These two voltages are $V_O R_2/(R_1 + R_2)$ and $V_{REF} + (V_{IN} - V_{SAT})R_4/(R_3 + R_4)$, respectively. When the voltage fed back via the negative-feedback loop approaches to voltage applied to the noninverting input of the amplifier, the output voltage of the amplifier will start to drop. This in turn will cause the voltage at point A to drop, and via the positive feedback loop, the voltage at the noninverting input terminal will also start to drop. This drop in the voltage at the noninverting input will accelerate the drop in the amplifier output voltage and thus in the drop in the voltage at point A. As a result of this positive-feedback condition Q_1 will rapidly be driven into cutoff.

With Q_1 in cutoff the output voltage will start to fall. As soon as the voltage fed back by the negative-feedback loop approaches the voltage at the noninverting input, the output of the amplifier will once again start to go up. This will cause Q_1 to turn on, raising the voltage at point A. This rise in voltage will be fed back to the amplifier via the positive feedback loop and accelerate the turn-on of Q_1, with Q_1 rapidly being driven into saturation. The output voltage will again start to go up and the cycle will then be repeated.

2.8.7 Switching Frequency

We will now derive an approximate expression for the switching frequency. We will first note that when Q_1 is on, the positive-feedback voltage will be $(V_{IN} - V_{SAT})R_4/(R_3 + R_4)$, where $V_{SAT} = V_{CE(SAT)}$ is the saturation voltage of Q_1. When Q_1 is off, the positive-feedback voltage will be $(-V_D)R_4/(R_3 + R_4)$, where V_D is the forward-bias voltage drop of D_1. The peak-to-peak swing in the positive-feedback voltage will therefore be $(V_{IN} - V_{SAT} + V_D)R_4/(R_3 + R_4) = V_{IN}R_4/(R_3 + R_4)$ since both V_{SAT} and V_D will have about the same value (0.7 V).

As a result of the switching action of Q_1, the output voltage will have some peak-to-peak ripple component. The switching of Q_1 via the amplifier occurs when the voltages at the two amplifier input terminals become equal to each other. Therefore, the peak-to-peak excursions in the positive-feedback voltage must be matched by an equal excursion in the negative-feedback voltage that is fed back to the inverting input of the amplifier via the R_1–R_2 voltage divider.

We will now turn our attention to the voltage fed back to the inverting input terminal via the negative-feedback loop. In addition to the d-c component of this feedback voltage there will be a small a-c component resulting from the a-c ripple on the output. Assuming a duty cycle of around 50% the input voltage can be considered to be a square wave with a peak amplitude of V_{IN}. The L_1–C_O network can

be considered to be a simple voltage divider for the a-c frequencies of interest with a voltage division ratio of

$$\frac{v_o}{v_A} = \frac{1/j\omega C_O}{j\omega L_1 + (1/j\omega C_O)} \simeq \frac{1}{\omega^2 L_1 C_O} \tag{2.102}$$

since $\omega L_1 \gg 1/\omega C_O$ for the frequencies of interest.

The voltage at point A can be analyzed using a Fourier series to give a d-c component, a fundamental term at the switching frequency and various odd harmonic terms. Due to the rapidly increasing attenuation of the L_1–C_O network with increasing frequency it will only be the fundamental term in the output that will be of any importance (except for the d-c term, of course). The fundamental term in the Fourier series has an amplitude given by $(2/\pi)V_{IN}$ at point A. At the output of the L_1–C_O low-pass filter the amplitude will be reduced by the factor $1/\omega^2 L_1 C_O$ to $v_o = (2/\pi)(1/\omega^2 L_1 C_O)V_{IN}$. The peak-to-peak voltage ripple at the output will therefore be twice this.

The peak-to-peak swing in the voltage fed back to the inverting input terminal of the amplifier will therefore be given by $(R_2/(R_1 + R_2))\ (4/\pi)(1/\omega^2 L_1 C_O)V_{IN}$. If we now equate the peak-to-peak voltage excursions at the amplifier input terminals, we obtain

$$\frac{V_{IN}(4/\pi)}{\omega^2 L_1 C_O} \frac{R_2}{R_1 + R_2} = V_{IN} \frac{R_4}{R_3 + R_4} \tag{2.103}$$

so that solving for ω, we obtain

$$\omega^2 = \frac{4/\pi}{L_1 C_O} \frac{R_2}{R_1 + R_2} \frac{R_3 + R_4}{R_4} \tag{2.104}$$

The switching frequency will therefore be given by

$$(2\pi f)^2 = \frac{4/\pi}{L_1 C_O} \frac{V_{REF}}{V_O} \frac{R_3 + R_4}{R_4} \tag{2.105}$$

after noting that $V_O R_2/(R_1 + R_2) = V_{REF}$. We see that the switching frequency will be a function of the $L_1 C_O$ product as well as the feedback factors for both the positive- and negative-feedback loops.

We will now consider a representative example and we will use some of the design specifications of the switching regulator considered previously: $I_O = 1.0$ A, $V_O = 10$ V, $V_{IN} = 20$ V, $f_s = 30$ kHz, and a ripple factor of 0.05%. To meet the ripple factor specification we obtained $L_1 = 500\ \mu$H and $C_O = 300\ \mu$F. We will now use these values to determine the values of R_3 and R_4 required to make this a self-oscillating regulator. We will assume a reference voltage of 1.8 V.

If we solve the equation above for the positive-feedback factor, $R_4/(R_3 + R_4)$, we obtain

$$\frac{R_4}{R_3 + R_4} = \frac{4/\pi}{\omega^2 L_1 C_O} \frac{V_{REF}}{V_O} \tag{2.106}$$

so that

$$\frac{R_4}{R_3 + R_4} = 4.3 \times 10^{-5}$$

Thus the positive-feedback factor required is extremely small. The small value of the positive-feedback factor is due in most part to the very small ripple factor. Indeed, the positive feedback factor can be obtained more directly by expressing the peak-to-peak negative-feedback excursion directly in terms of the ripple factor as $rV_OR_2/(R_1 + R_2)$, where r is the peak-to-peak ripple factor. Since $V_OR_2/(R_1 + R_2) = V_{REF}$, this can be rewritten as rV_{REF}. Thus the peak-to-peak excursion in the negative-feedback voltage is simply equal to product of the ripple factor and the reference voltage. Since the peak-to-peak excursion in the positive-feedback voltage has previously been given as $V_{IN}R_4/(R_3 + R_4)$, we can now obtain the equation for the required positive-feedback factor by equating the two peak-to-peak excursions giving $V_{IN}R_4/(R_3 + R_4) = rV_{REF}$, so that $R_4/(R_3 + R_4) = rV_{REF}/V_{IN}$.

If we use a ripple factor of 0.05%, a reference voltage of 1.8 V, and an input voltage of 20 V, we obtain a positive-feedback factor of 4.5×10^{-5}, which is essentially the same as obtained previously. If R_4 is the source resistance of the voltage reference circuit of 1 kΩ, the value of $R_3 + R_4$ will be 22 MΩ, so that R_3 will be essentially 22 MΩ.

In practice, a ripple factor as low as 0.05% may be very difficult to achieve in a switching regulator due to the effects of the capacitor series resistance (ESR). In practice, a ripple factor in the range of 0.1 to 1% may be the best that can be achieved. For a ripple factor of 1%, the calculations above would yield a positive-feedback factor of 9×10^{-4}, so that R_3 would now be 1.1 MΩ.

One of the principal disadvantages of the switching type of voltage regulator in comparison to the linear or nonswitching type (i.e., the dissipative type) is the greater ripple factor present at the output of the switching regulator. With the linear regulator the output ripple is reduced below the input ripple level by the ripple rejection factor of the regulator. This factor is typically in the range 60 to 80 dB. For example, if the input ripple is 1% and the ripple rejection factor is 60 dB, the output ripple will be only 0.001%.

On the other hand, it must be understood that in the switching regulator the output ripple is due principally to the switching action of the regulator itself and is not due to the feedthrough of ripple from the input circuit. As a result of this a smaller filter capacitor and inductor can be used in the rectifier power supply that provides the input voltage for the switching regulator. In addition, the output ripple that does result is at a relatively high frequency, typically in the range 20 to 50 kHz as compared to the predominant output ripple component of 120 Hz for the linear type of regulator. The higher ripple frequency of the switching regulator can much more easily be filtered than that of the linear regulator by the use of low-pass filters or bandpass filters at various critical points in the circuits that are supplied by the regulator. Furthermore, with the driven switching regulator it is possible to synchronize the switching rate with some other frequency in the system supplied by the regulator such that the ripple is less of a problem.

2.8.8 Examples of Switching Regulator Circuits

We will now consider some examples of switching regulator circuits starting off with the externally driven regulators. The externally driven regulators offer the advantage of operating at a fixed switching frequency that is independent of line and load conditions. This fixed switching frequency can be chosen so as to optimize performance of the regulator. The disadvantage of the externally driven regulator is, of course, the necessity of proving for a square-wave oscillator circuit to drive the regulator.

In Figure 2.31 a circuit diagram is present of an adjustable voltage regulator that is connected as an externally driven switching regulator. The voltage regulator itself can be any of the LM105 or LM376 type, and is similar to that presented in Figure 2.12. The current boost circuitry consisting of Q_1 and Q_2 and R_5 is the same as for the linear regulator circuit. Resistor R_4 is used for current limiting, and there is a feedback of a portion of the output voltage via the R_1–R_2 voltage divider to the inverting input of the error amplifier (pin 6).

The square-wave input is integrated by the R_3–C_3 network to become a triangular waveform that is applied to the noninverting input of the error amplifier (pin 5). The internally generated reference voltage is also applied to this amplifier input so

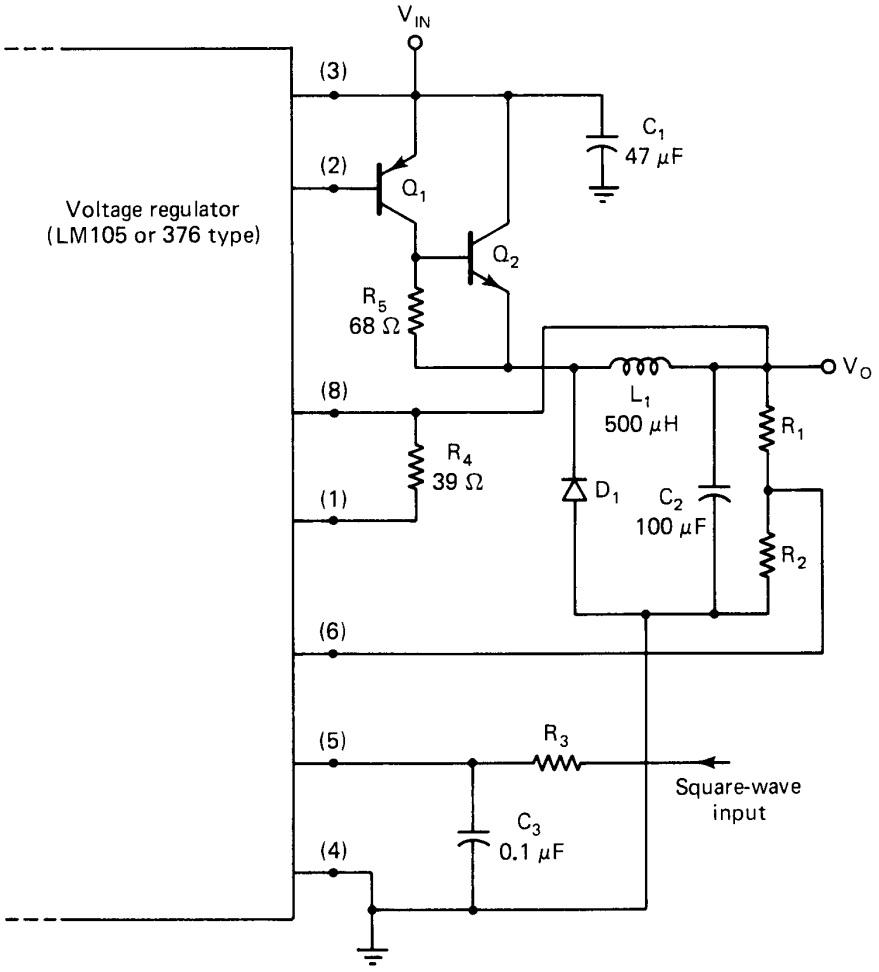

Figure 2.31 Switching regulator driven by external square-wave generator.

that the total instantaneous voltage consists of a small-amplitude triangular waveform superimposed on the reference voltage as shown in Figure 2.32. The peak-to-peak excursion of the triangular waveform is typically about 40 mV for the best performance of the circuit.

With the input voltages just described, the error amplifier operates as a pulse-width modulator. The two input voltages of the error amplifier are shown in Figure 2.32. The output of the error amplifier will be in the high state whenever $V_{REF} + v_{triangular}$ is greater than the feedback voltage, $V_{FB} = V_O R_2/(R_1 + R_2.)$ When this happens Q_1 and Q_2 will be turned on (in saturation). Conversely, when $V_{REF} + v_{triangular}$ is less than V_{FB}, the error amplifier output will be in the low state and Q_1 and Q_2 will be off. We therefore see that the series-pass transistors will be turned on and off every cycle of the input square wave. The duty cycle, $\delta = t_{on}/T$, will be a function of the value of V_{FB} relative to V_{REF}.

Under steady-state equilibrium conditions, the duty cycle will be adjusted by the feedback loop at the value necessary to maintain the desired output voltage. For example, if $V_{IN} = 20$ V and V_O is to be 5 V, a duty cycle of approximately 25% is required, essentially as is shown in Figure 2.32. Assuming a reference voltage

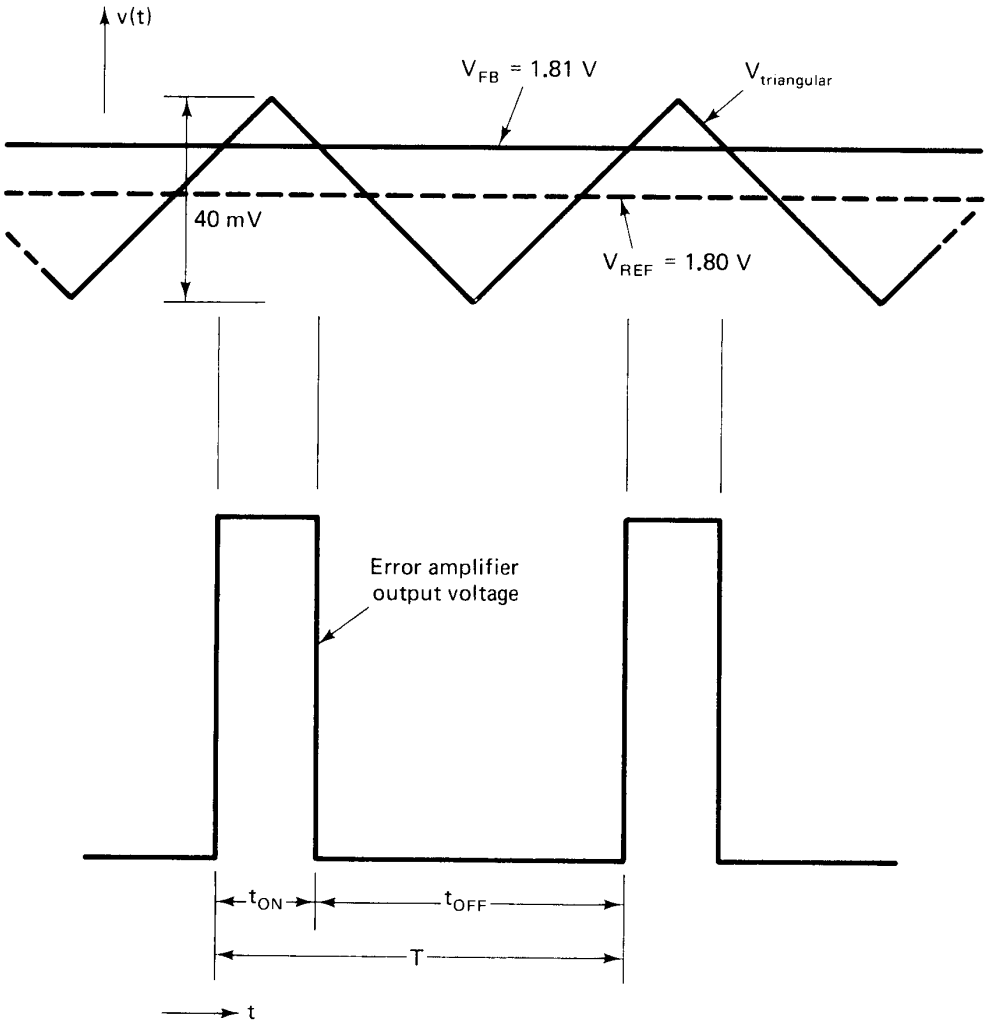

Figure 2.32 Voltage waveforms for driven switching regulator.

of $V_{REF} = 1.80$ V and a 40 mV peak-to-peak swing for the triangular waveform, the value of V_{FB} under equilibrium conditions will be $V_{FB} = V_{REF} + 10$ mV = 1.81 V. For a 5.0-V output, the required resistance ratio will be given by the equation $(5.0 \text{ V})(1 + R_1/R_2) = V_{REF} + 10 \text{ mV} = 1.81$ V.

Now if for some reason, such as an increased load current or a drop in line voltage, the output voltage drops below 5.0 V, we see that the duty cycle will lengthen and become greater than 25%. The increased duty cycle will bring V_O up back toward 5.0 V. Conversely, if for some reason, such as a sudden drop in load current V_O goes above 5.0 V, we see that the duty cycle will shorten to less than 25%. The shorter duty cycle will act to bring V_O back toward the 5.0-V equilibrium level.

We see from this example that the triangular waveform input will produce, in effect, a small shift in the reference voltage. In the example above, with a 25% duty cycle, a 10-mV shift resulted. For this reason, and the fact that the amplitude of the triangular waveform may not be temperature-compensated or well regulated, an excessively large peak-to-peak amplitude for the triangular waveform is to be avoided. On the other hand, too small an amplitude for the triangular waveform may allow the circuit to go into self-oscillation. The peak-to-peak amplitude of the triangular wave should usually be in the range 10 to 100 mV, with 40 mV generally being about the optimum value.

Self-oscillating switching regulator. A diagram of a self-oscillating switching regulator is presented in Figure 2.33. The connections shown are made to a linear voltage regulator of the LM105 or LM376 type. Most of the circuitry is the same as for the externally driven regulator that has just been discussed. The principal difference has to do with the signal fed to the noninverting input of the error amplifier (pin 5). In the externally driven regulator this was a triangular waveform obtained by the integration of a square wave input. In the self-oscillating regulator it is obtained from the emitter of Q_2 via resistor R_3. It is this connection that provides the positive feedback that is necessary to sustain oscillations.

The resistance seen looking into pin 5 is essentially the source resistance of the voltage reference of about 1 kΩ. Therefore, the positive feedback factor is approximately 1 kΩ/1 MΩ = 0.001.

From the analysis of the self-oscillating switching regulator we have obtained the simple relationship between the output ripple factor r and the positive-feedback factor as given by

$$\frac{rV_{REF}}{V_{IN}} = \frac{R_4}{R_3 + R_4} = \text{positive-feedback factor} \tag{2.107}$$

Now if for an example we let $V_{IN} = 20$ V and $V_{REF} = 1.8$ V, and for the moment neglect the effect of C_3, we have that

$$r\left(\frac{1.8}{20}\right) = \frac{1\text{k}\Omega}{1\text{M}\Omega} = 0.001 \tag{2.108}$$

so that the ripple factor will be r = 1.1%.

We will now consider the effect of C_3. Capacitor C_3 will, of course, have no influence on the d-c output voltage. If, however, the reactance of C_3 is small compared

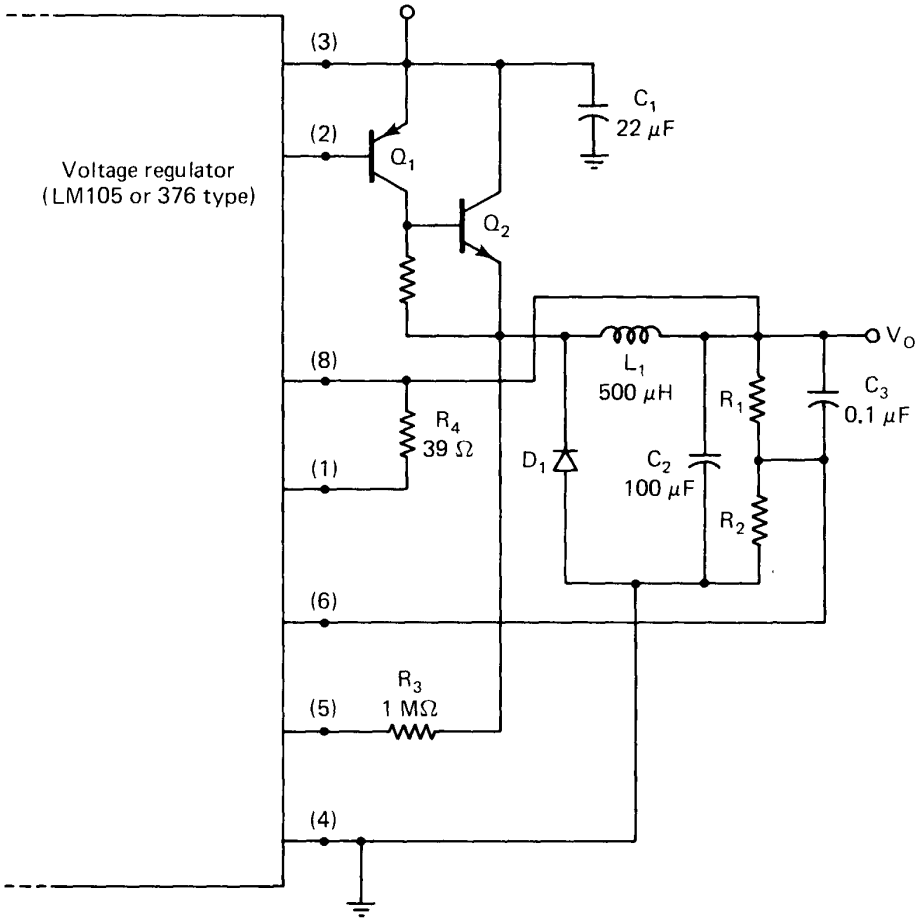

Figure 2.33 Self-oscillating switching regulator.

to the resistance of R_2, then almost the full a-c ripple voltage will appear at the noninverting amplifier input (pin 6). We must accordingly modify the relationship used above. Since the peak-to-peak excursion at pin 5 will be $V_{IN}R_4/(R_3 + R_4)$, and that at pin 6 will now be given by rV_O, we will have that

$$r\frac{V_O}{V_{IN}} = \frac{R_4}{(R_3 + R_4)} \tag{2.109}$$

Assuming an output voltage of 10 V, the ripple factor becomes

$$r = 0.001 \times \frac{20\text{ V}}{10\text{ V}} = 0.002 \quad \text{or} \quad \underline{0.2\%} \tag{2.110}$$

In practice this low a value for the ripple factor may be difficult to achieve due to the effects of the capacitor (C_2) effective series resistance.

With this type of regulator operating at an output voltage of 10 V and input voltages in the range 13 to 40 V, efficiencies in the range 85 to 90% are obtainable at an output current level of 1 A. As the output current increases, the efficiency will decrease slowly as a result of the increasing I^2R losses in the inductor and in the transistor, but even at 5-A output current the efficiency will still be up at around 72% with $V_{IN} = 28$ V.

With the component values as shown in Figure 2.32, the switching frequency will range from about 20 kHz at an output current of 0.5 A to 40 kHz at 5.0 A. The change in the switching frequency is due in large part to the decrease in the inductance of the coil with increasing current resulting from the effects of magnetic saturation of the inductor core.

2.8.9 Regulating Pulse-Width Modulator

Another switching voltage regulator that is worthy of mention is the 1524/2524/3524 (National Semiconductor, Signetics, Silicon General, etc.) type of regulating pulse-width modulator. This device is basically a switching voltage regulator with an on-chip oscillator circuit and so can be connected as a driven switching regulator without the need of any external oscillator. The frequency of oscillation is set by an external resistor and capacitor from as low as 1 kHz up to a maximum of 350 kHz.

This regulator can be connected in a variety of configurations as a step-down or as a step-up switching regulator, and with or without current boosting using external series-pass transistors.

When used as a 1-A 5-V step-down regulator with $V_{IN} = 10$ V at a 20 kHz switching frequency an efficiency of 80% is obtainable. The ripple will be 10 mV peak-to-peak, corresponding to a ripple factor of 0.2%. The load regulation for a variation in the output current of from 200 mA to 1 A will be 3 mV, corresponding to 0.06%/V. The line regulation will be 6 mV for an input voltage change of from 10 to 20 V, corresponding to a line regulation factor of 0.12%/V.

A similar type of pulse width modulator control circuit is the MC34060/35060 (Motorola). This IC contains an oscillator, 5.0 V reference, comparator, and error amplifier and can be used for step-down, step-up, and inverting voltage regulator circuits.

2.8.10 Monolithic Switching Regulator

An example of a monolithic switching regulator is the LAS6320P made by Lambda Semiconductors. This device comes in a 14-pin DIP package and contains a temperature-compensated voltage reference, sawtooth oscillator, pulse width modulator, error amplifier, and a Darlington output transistor with a 2 A rating and internal current limiting protection. The internal reference voltage is 2.25 V, the error amplifier has an open loop gain of 70 dB, and the output section current limit is set at 2.8 A. Maximum ratings include an input voltage of 35 V, and an oscillator frequency of 200 kHz. The junction-to-case and case-to-ambient (free air) thermal resistances are 13°C/W and 47°C/W, respectively, Typical performance characteristics include a line regulation of 0.015%/V and an output voltage temperature coefficient of 0.01%/°C. Both step-down and step-up modes of operation are possible. When operated as a step-down regulator with $V_{in} = 24$ V, $V_o = 5$ V, and an oscillator frequency of 50 kHz, the system conversion efficiency is 72% at an output current of 0.5 A, and is 76% for an output current of 2 A. For an output voltage of 12 V and an output current of 2 A, the efficiency will be up to 85%.