Spicing-Up Spice II Software For Power MOSFET Modeling

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The SPICE II simulation software package is familiar to most designers working in computer-aided design of integrated circuits. Developed by L. W. Nagel in 1973, SPICE II has become a widely available, well-understood design tool for IC modeling and analysis. But, SPICE II has a shortcoming: its standard simulation programs were developed when all MOSFETs were low-power devices. Power MOS devices are growing in use today, both as discrete components and, potentially, as output stages of power integrated circuits. SPICE II in its current form doesn't recognize these new developments. Its built-in FET models aren't able to simulate all the modes of new power MOS device operation. For example, SPICE II doesn't recognize the way a power MOSFET's internal capacitances change with bias conditions, the presence of a cascode JFET that complicates both static and dynamic operation, or the presence of a parasitic body diode that affects operation in the third quadrant. Without this information, SPICE II will predict power MOSFET performance that is incorrect.

Since SPICE II's internal device models can't be easily changed for all existing copies, we looked for another approach to update the capabilities of this widely used simulation package in its standard form. Adding a "subcircuit" of external components that complement the devices within the SPICE II software, so as to form a true, equivalent circuit of a power MOSFET, is the answer.

The subcircuit works nicely with the standard SPICE II software, providing a model with all the terminal characteristics of a power MOSFET. Parameters of the subcircuit model can be determined from simple terminal measurements or from standard data sheets, using the algorithmic and empirical approach described below. Once these parameters are in place, SPICE II can be used to accurately simulate either p-channel or n-channel power MOSFET devices over a wide range of currents and voltages. The subcircuit functions as an embedded subroutine, so it can be used repetitively for any number of power MOSFETs in a design. This technique can be used to model power MOSFETs with any version of the SPICE II program presently available, without any modifications to its internal source code. The technique can also be used with other commercially available or in-house-developed circuit simulators.

Modeling The Power MOSFET

A cross-sectional view of a cell of a Intersil IRF130 power MOSFET is shown in Figure 1. The easiest way to understand its electrical characteristics is to think of it as a vertical JFET, driven in cascode from a low-voltage lateral MOSFET.[1, 2] When the gate is positively biased with respect to the n-bulk, an accumulation layer forms in the n-region beneath the gate. This layer acts as the drain of the lateral MOSFET, as well as the source of the vertical JFET. The JFET channel is then-region between the two p-type body diffusions, which act as the gate of the JFET. The JFET drain is the n+ bulk, usually thought of as the power MOSFET drain.

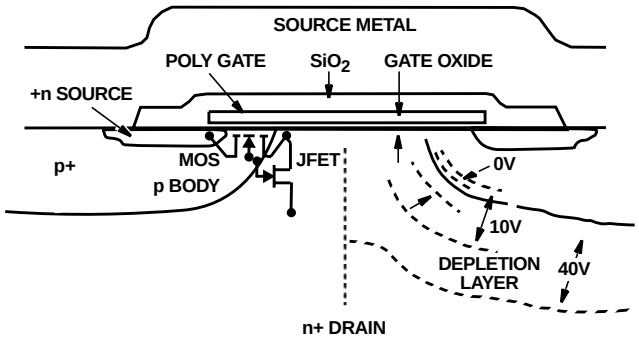

FIGURE 1. A CROSS-SECTIONAL VIEW SHOWS THE PHYSICAL MAKEUP OF THE LATERAL LOW-VOLTAGE MOSFET AND VERTICAL JFET THAT OPERATE IN CASCODE AS THE POWER MOSFET.

When you look at the power MOSFET this way, it becomes possible to use the standard SPICE II built-in device models, because SPICE II can simulate both the vertical JFET and the lateral MOSFET. When we use the subcircuit to add the rest of the Intersil IRF130 power MOSFET to these SPICE II-simulated devices, we get a satisfactory equivalent circuit, shown in Figure 2.

The gate-to-source capacitance of the Intersil IRF130 power MOSFET is represented by C_{21}. It is really a composite of two capacitances. The first is formed between the polysilicon gate and source metal (with the thick oxide as a dielectric). The second is formed between the gate and the n+ source (with the thin oxide acting as the dielectric). The value of C_{21} is essentially unchanged by voltage or current.

Capacitor C_{24} is formed between the power MOSFET gate and the accumulation layer, with the thin gate oxide as a dielectric. So long as the gate is positive with respect to the n-neck region, the accumulation layer exists and C_{24} doesn't change. But, if the external drain voltage (less their voltage drop across then-drift region) approaches the gate voltage, the accumulation layer starts to disappear. When that happens, C_{24} abruptly drops in value. This sudden change has to be taken into consideration.

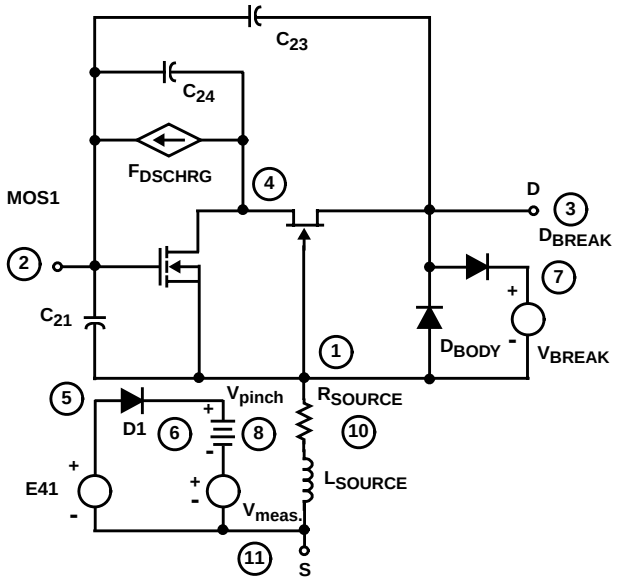

FIGURE 2. THE EQUIVALENT CIRCUIT OF THE POWER MOSFET IS MADE BY COMBINING SPICE II MODEL ELEMENTS WITH SOFTWARE SPECIFIED COMPONENTS ON A "SUBCIRCUIT."

Capacitor C_{23} represents the gate-to-drain capacitance of the Intersil IRF130 power MOSFET. Because the accumulation layer normally acts as an electrostatic shield, C_{23} has no significance until the layer ceases to exist under the conditions just described. When it does disappear, the effect upon C_{23} is abrupt, and also has to be taken into consideration. The sudden changes in C_{24} and C_{23} cannot be easily modeled with the standard SPICE II software.

Figure 2 illustrates what happens: If the JFET source voltage (node 4) is very low compared to its pinch-off voltage, the JFET will be highly conductive, tightly coupling C_{24} to the JFET drain (which is also the drain of the Intersil IRF130 power MOSFET). However, as the node 4 voltage approaches the pinch-off voltage (V_{PINCH}) of the JFET, it operates in a constant-current mode. This action decouples C_{24} from the JFET drain, making possible a much faster slew-rate, determined by C_{23}. If the node 4 voltage is allowed to exceed V_{PINCH} of the JFET, errors will exist in the output waveforms predicted by the standard SPICE II model.

To correct the situation, the added subcircuit includes a current-controlled current source, F_{DSCHRG}, and a current-sense network containing D1. If node 4 voltage begins to exceed V_{PINCH} of the JFET, D1 conducts, and its current is sensed at V_{MEAS}. The high-gain current source F_{DSCHRG} is turned-on rapidly and partially discharges C_{24}, pinning node 4 voltage at the pinch-off voltage of the JFET. In setting up the parameters of the subcircuit, the ideality factor of D1 is set at 0.03 to assure that node 4 voltage will never exceed V_{PINCH} of the JFET by more than a few millivolts. This condition results in waveform predictions from the SPICE II model that represent the true characteristics of the power MOSFET.

The body diode (D_{BODY} in Figure 2) is formed by the drain-to-body diffusion pn junction of the Intersil IRF130 power MOSFET. D_{BODY} is added as an external component in the subcircuit because the built-in gate-to-drain diode of the SPICE II JFET model is inconvenient when it comes to modeling third-quadrant conduction of a power MOSFET. We want most of the third-quadrant current to flow in D_{BODY}. So, we effectively delete the SPICE II model's built-in diode by setting its saturation current parameter to an artificially low value, such as 10^{-20} ampere.

To round-out the subcircuit, a resistor value is chosen for the JFET drain of the SPICE II model to represent the series resistance of the n-drain region of the Intersil IRF130 power MOSFET.[3] We also add resistor R_{SOURCE} to represent the series source resistance of the Intersil IRF130 power MOSFET: a composite of resistances in the n+ source region, contact resistance, and source-metal series resistance. Finally, we add inductor L_{SOURCE} to represent the source inductance of the power MOSFET contributed by the source metallization and bond wires.

Choosing Parameters to Simulate A Power MOSFET

To accurately simulate the terminal characteristics of the physical power MOSFET you are working with, you will need to adjust the SPICE II model parameters and select subcircuit component values. Look first at adjustment of the SPICE II model. The static current-voltage characteristics of the power MOSFET are determined by the low-voltage lateral MOSFET included in the SPICE II model; Figure 2. In saturation (large values of V_{DS}), the lateral MOSFET device is modeled according to the following equation:

$$I_{DS} = \frac{(K_P)W\,(V_{GS} - V_{TO})^2}{2L}$$

where

K_P = Process Transconductance Parameter

V_{TO} = Threshold Voltage

W = L = 1µm (Fixed In This Note For Convenience)

I_{DS} = MOSFET Drain Current

V_{GS} = MOSFET Gate-To-Source Voltage

Continuing with the example device, the Intersil IRF130 power MOSFET, a plot of the square root of I_{DS} versus gate voltage (V_{GS}) provides the curves shown in Figure 3 for V_{DS} = 10 volts. These curves provide the process transconductance parameter, $(K_P/2)^{0.5}$, and threshold voltage, V_{TO}, directly. This data can then be used to find the value of source resistance, R_{SOURCE}. This series resistance is important because it causes the curve produced by plotting the square root of I_{DS} versus V_{GS} to depart from linearity at high current levels. Departure at very low current levels is caused by subthreshold conduction, which we ignore in this model.

To find the JFET drain resistance, we use the value of source resistance, R_{SOURCE}, and plots of I_{DS} versus V_{DS} for operation in the linear region, as shown in Figure 4.

To find the current, resistance and capacitance parameters of the body diode (D_{BODY} in Figure 2), first plot log I_{DS} versus V_{DS}, as shown in Figure 5, holding the gate voltage, V_{GS}, negative for third-quadrant operation; i.e., where V_{DS} is less than 0. This plot gives the saturation current and resistance of D_{BODY}. The minority-carrier transit-time parameter (TT) of the SPICE II program is chosen to provide the best fit to measured transient reverse-recovery data. The junction capacitance value of D_{BODY} is equal to the power MOSFET device output capacitance, C_{OSS}, at zero volts. This value can be obtained from the device data sheet, or by bridge measurement. It is usually specified at 25 volts, and may be converted to zero volts by multiplying by 6.

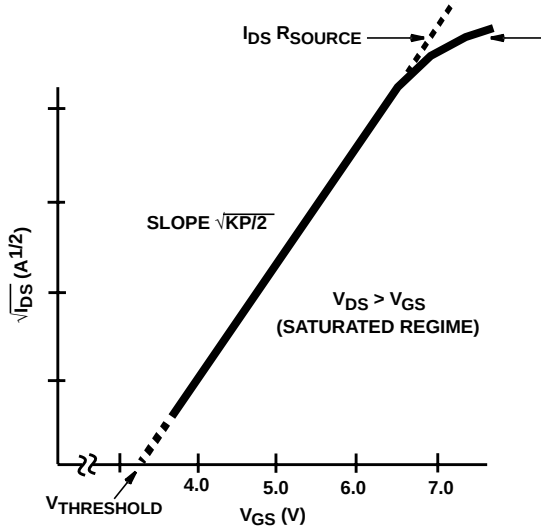

FIGURE 3. THIS PLOT OF THE SQUARE ROOT OF DRAIN CURRENT vs. GATE VOLTAGE DEFINES THE THRESHOLD VOLTAGE, V_{TO}, $(K_P/2)^{0.5}$, AND R_{source}, FOR THE POWER MOSFET.

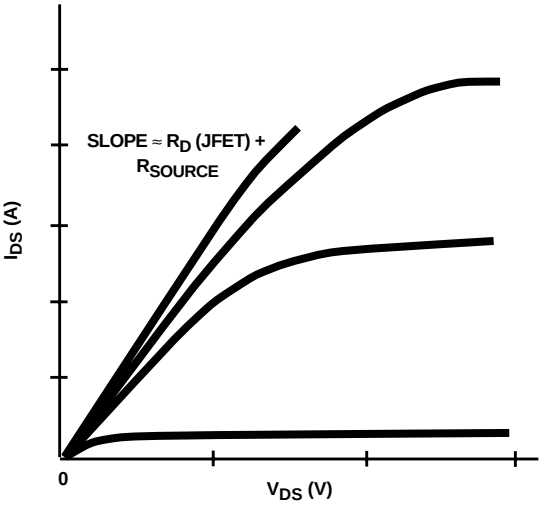

FIGURE 4. DRAIN CURRENT vs. DRAIN VOLTAGE OF THE POWER MOSFET PLOTTED USING CONSTANT GATE VOLTAGES. THIS CURVE DEFINES THE ON RESISTANCE OF THE DEVICE.

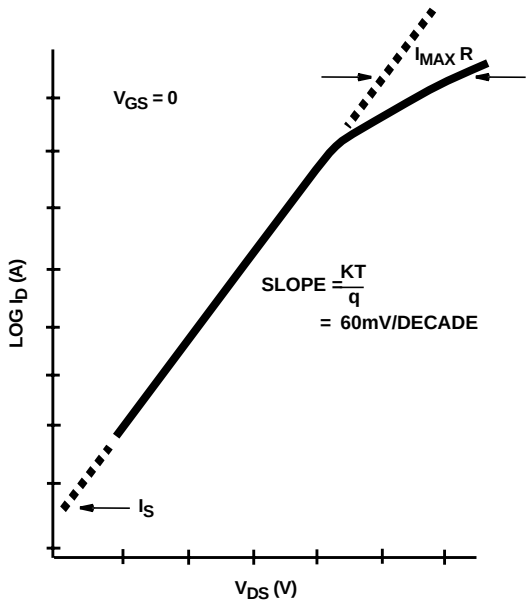

FIGURE 5. THIS PLOT OF LOG I_D VS V_{DS} IN THIRD-QUADRANT OPERATION OF THE POWER MOSFET DEFINES I_S AND R_S, OF THE PARASITIC BODY DIODE, D_{BODY}.

To properly simulate avalanche breakdown voltage with the added clamp circuit (diode D_{BREAK} and voltage source V_{break} in Figure 2), first set the voltage level of V_{BREAK} equal to the measured value of drain breakdown voltage. Then, adjust the SPICE II model parameters I_S, N, and R_S for D_{break} to obtain the best fit to the measured breakdown voltage curve.

Selection of capacitors C_{21}, C_{23}, and C_{24}, and the parameters of the JFET (all shown in Figure 2), can be made using the curves of Figure 6. This is a plot of drain and gate voltage versus time for a power MOSFET driven with constant

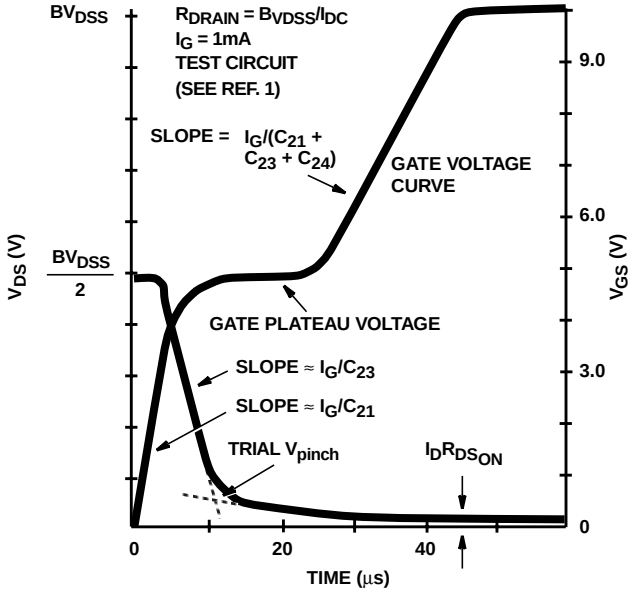

FIGURE 6. PLOTTING DRAIN AND GATE VOLTAGES OF THE POWER MOSFT VS TIME DETERMINES THE VALUES OF C_{21}, C_{23}, C_{24}, AND V_{pinch}.

gate current (I_G).[1] The initial slope of the V_{GS} curve defines C_{21} (since for any value of gate voltage, V_{GS}, less than threshold voltage, V_{TO}, the power MOSFET is in its off-state, so that the gate-to-source capacitance, C_{21}, charges linearly under constant-current conditions). As V_{TO} is reached, the low-voltage lateral MOSFET (Figure 2) turns on, and its drain voltage drops toward its minimum value.

At the outset, the JFET is operating beyond pinch-off, and the slope of the V_{DS}-versus-time curve is controlled by C_{23}. However, when the drain voltage falls below V_{PINCH}, the JFET conducts, strongly coupling C_{24} to the JFET drain and greatly reducing the drain voltage slew rate. Thus, the value of C_{23} can be approximated from the steep slope of the VDS curve in Figure 6, while the value of C_{21}+C_{23}+C_{24} corresponds to the labelled V_{GS} slope. These values can be adjusted slightly to give the best slope fit. A trial value of V_{PINCH} (and V_{TO}) is given by the labelled intercept of the V_{DS} curve. Adjustments of this value will control the length of the gate plateau voltage needed to complete the curve fit.

Table I lists the preferred algorithm for parameter extraction; Table II summarizes the required empirical inputs. Together, these tables will aid in setting up the parameters for evaluation of a power MOSFET with SPICE II and the subcircuit. As an example, Table 3 summarizes the input parameters for the SPICE II model and subcircuit, determined for the Intersil IRF130 power MOSFET, using the approach just described. The IRF130 is rated at 14 amperes and has a 100-volt blocking capability.

TABLE 1. PREFERRED ALGORITHM FOR PARAMETER EXTRACTION

1.	Determine K_P of lateral MOS
2.	Determine V_{TO} of lateral MOS
3.	Determine C_{21}
4.	Determine $C_{21} + C_{23} + C_{24}$
5.	Determine Rsource and JFET drain resistance
6.	Assign beta of JFET = 100 x K_P of lateral MOS
7.	Use trial V_{PINCH}
8.	Use trial C_{23} and calculate C_{24}
9.	Curve fit for slope by repeating step 8 with different values of C_{23}.
10.	Adjust V_{PINCH} and V_{TO} of JFET to fix gate-voltage plateau

TABLE 2. EMPIRICAL INPUTS

MOSFET	Enhancement mode:W = L = 1µm; K_P (Figure 3); V_{TO} (Figure 3); C's = 0; T_{OX} = 1E6µm
JFET	Depletion mode; area factor = 1; Beta = 100K_P (Figure 3); V_{TO} = -V_{pinch} (Figure 6); C's = diode lifetime = 0; diode ideality factor = 1.0; Is = 1E - 20; R_D (Figure 4)
D_{BODY}	I_S from Figure 5; Ideality Factor = 1.0; R_S from Figure 5 (must be very much smaller than R_D); C (from C_{OSS}); lifetime = best fit to T_{RR}

TABLE 2. EMPIRICAL INPUTS (Continued)

D_{BREAK}	I_S = arbitrary; C = lifetime = 0; ideality factor = best low-current fit; R = best high-current fit
D1	I_S = 1E - 13; C = lifetime = 0; ideality factor = 0.03; R_S = 1
R_{SOURCE}	Figure 3
L_{SOURCE}	Approx. (5L)In(4L/d) nH; L and d are source wire inches
V_{PINCH}	Figure 6
V_{BREAK}	Avalanche voltage
C_{21}	Figure 6
C_{23}	Figure 6
C_{24}	Figure 6

TABLE 3 - INPUT PARAMETERS OF IRF130 TO SPICE MODEL

SPICE PARAMETER	INTERSIL IRF130 VALUE
LATERAL MOS	
Model Level	1
T_{OX}	1E06µ
V_{TO}	3.4V
K_P	6.4A/V^2
W, L	1.0µ
VERTICAL JFET	
JMOD Area	1
V_{TO}	-6.4V
Beta	640
I_S	10^{-20}
R_D	42.15 x $10^{-3}\Omega$
D_{BODY}	
CJO	1650pF
IT	70 x 10^{-9}
I_S	3 x 10^{-12}
R_S	2.5 x $10^{-3}\Omega$
PASSIVE ELEMENTS	
C_{21}	900pF
C_{23}	40pF
C_{24}	1360pF
R_{SOURCE}	17.5 x $l0^{-3}\Omega$
L_{SOURCE}	7.5 x 10^{-9}H
V_{BREAK}	117V

Implementing The Subcircuit in SPICE II

Table IV is the input listing for the implementation of the power MOSFET subcircuit in SPICE II software. Nodes are identified for drain, gate, and source of the power MOSFET. The subcircuit then "hooks" to these nodes wherever specified in the SPICE II simulation. Any number of power MOSFETs can be specified. The parameters listed are for an IRF130 power MOSFET.

The Results

The real test of the enhanced SPICE II model is how closely its predicted performance compares with actual measurements. Using the input parameters for the Intersil IRF130 device example given in Table III, we calculated transfer and output curves for the model. These curves were then compared against measured static data. Figures 7 and 8 show the precise fit between predicted and measured static data, even at low values of drain voltage.

To see how the model performs in dynamic prediction, we simulated first-quadrant operation (including avalanche mode) and third-quadrant operation for the Intersil IRF130 power MOSFET. Once again, the predicted performance of the enhanced SPICE II model fits actual measurements satisfactorily over the entire operating range of the Intersil IRFl30, as shown in Figures 9 and 10.

To compare calculated switching performance versus actual measurement on the Intersil IRF130, we used the enhanced SPICE II model to generate switching curves. Figure11 shows drain and gate voltages versus time with a constant gate-current drive. Figure 12 shows drain and gate voltages.

TABLE 4 - INPUT LISTING OF SUBCIRCUIT MODEL

Listed Parameters Valid for a Intersil IRFl30 Power MOSFET

```
* THIS IS THE POWER MOS SUBCIRCUIT
* NODE 3 IS THE POWERMOS DRAIN
* NODE 2 IS THE POWERMOS GATE
* NODE 11 IS THE POWERMOS SOURCE
*
*
.OPTIONS NOMOD NOLIST NOACCT NONODE LIMPTS=250 GMIN=1.0E-20
.SUBCKT POWMOS 3 2 11
C21 2 1 900P
C23 2 3 40P
C24 2 4 1360P
FDSCHRG 4 2 VMEAS 1.0
MOS1 4 2 11 MOSMOD L=1U W=1U
JFET 3 1 4 JMOD AREA=1
DBODY 1 3 DMOD2
RSOURCE 1 10 17.5E-03
LSOURCE 10 11 7.5N
E41 5 11 4 1 1.0
D1 5 6 DMOD
VPINCH 6 8 DC 6.4
VMEAS 8 11 DC 0.0
DBREAK 3 7 DMOD3
VBREAK 7 1 DC 117
.MODEL MOSMOD NMOS VTO=3.4 KP=6.40 TOX=1.0E+06U
.MODEL JMOD NJF VTO=-6.4 BETA=640 IS=1.0E-20 RD=42.5E-03
.MODEL DMOD D IS=1.0E-13 N=0.03 RS=1.0
.MODEL DMOD2 D CJO=1650P TT=70N IS=3.0E-12 RS=2.5E-03
.MODEL DMOD3 D IS=1E-13 RS=2.0 N=1.0
.ENDS
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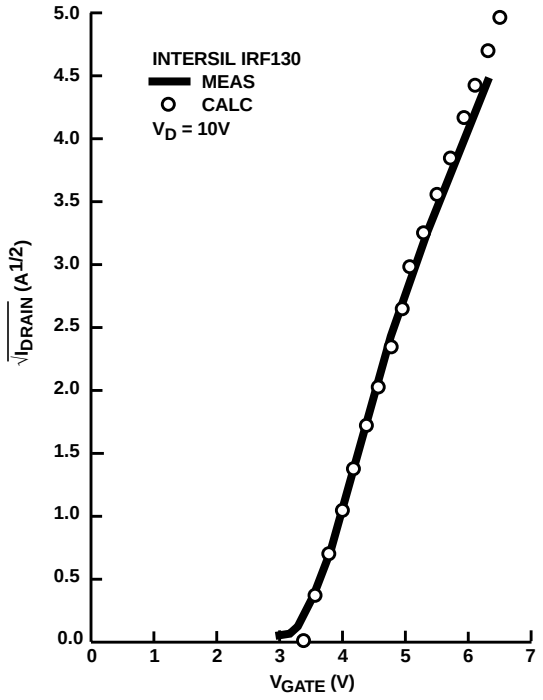


FIGURE 7. MEASURED SQUARE ROOT OF DRAIN CURRENT (DRAIN VOLTS = 10) vs. GATE VOLTAGE FOR THE INTERSIL IRF130 POWER MOSFET IS PLOTTED ALONG WITH THE CALCULATED VALUES FOR THE ENHANCED SPICE II MODEL. AN EXCELLENT FIT IS OBTAINED.

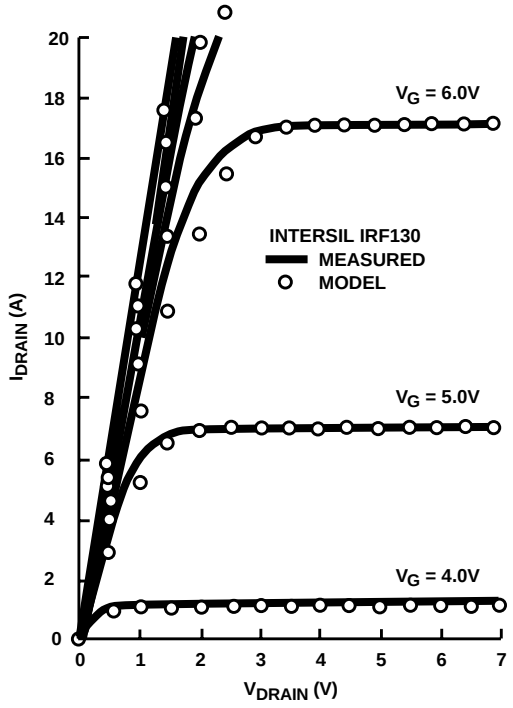


FIGURE 8. PLOTS OF DRAIN CURRENTvs. DRAIN VOLTAGE FOR THE INTERSIL IRF130 POWER M0SFET SHOW AN EXCELLENT FIT BETWEEN MEASURED VALUES AND THOSE CALCULATED BY THE ENHANCED SPICE II MODEL FOR VARIOUS VALUES OF CONSTANT GATE VOLTAGE.

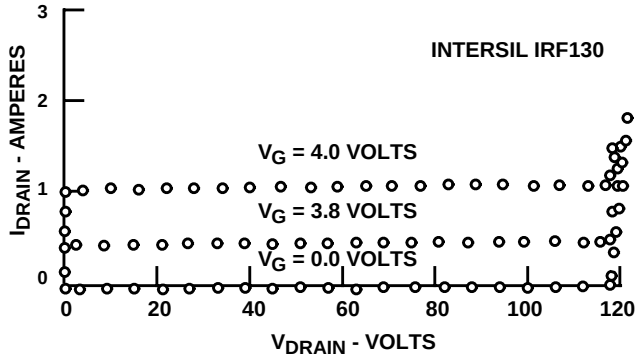


FIGURE 9. FIRST QUADRANT DRAIN CURRENT vs. DRAIN VOLTAGE WITH V_{GS} HELD CONSTANT IS CALCULATED BY THE ENHANCED SPICE II MODEL OF THE INTERSIL IRF130 POWER M0SFET. NOTE THAT THE MODEL PREDICTS AVALANCHE BREAKDOWN.

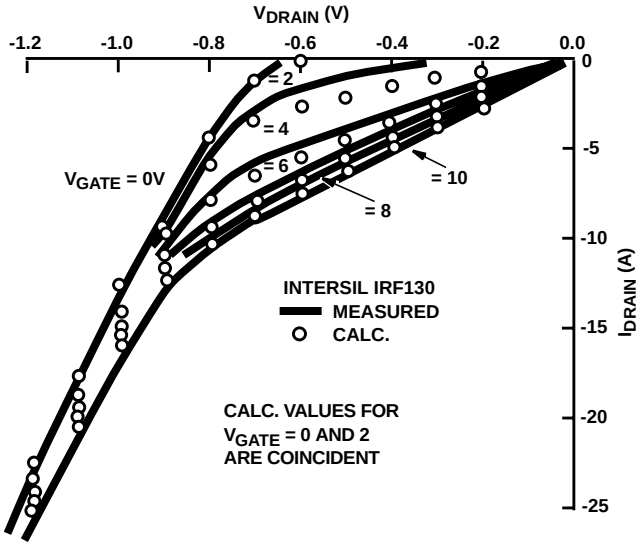
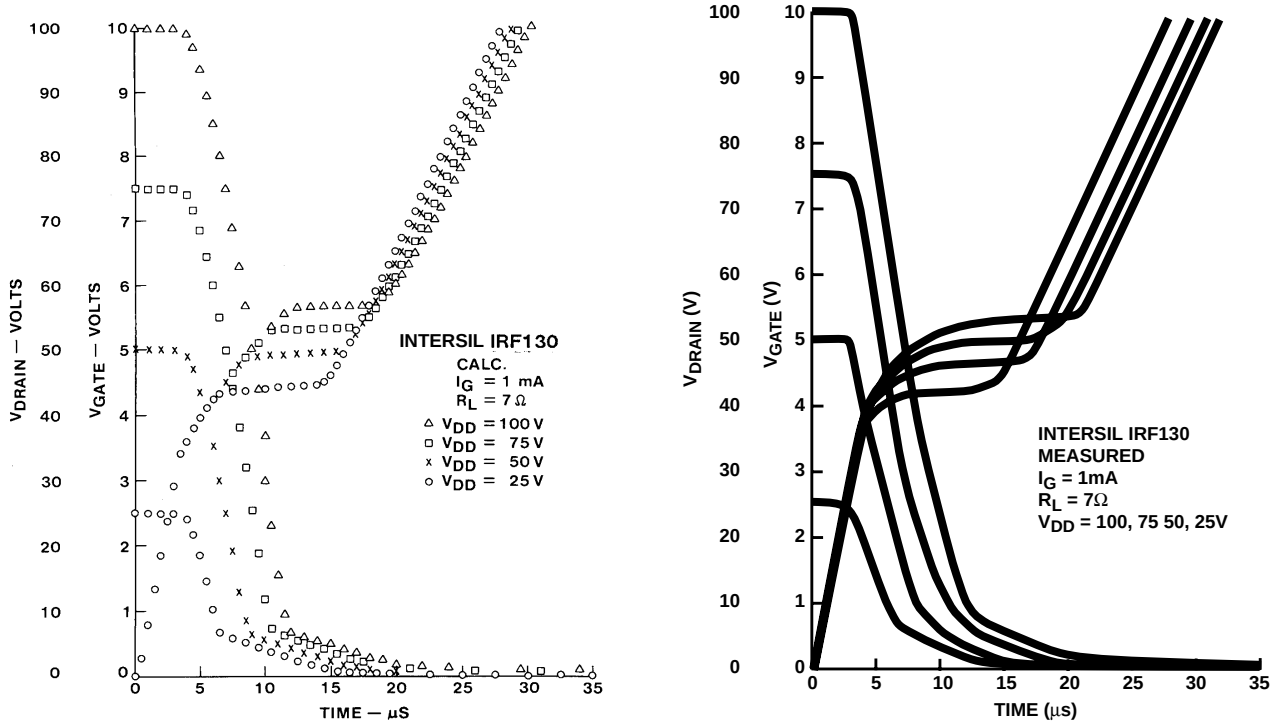


FIGURE 10. THIRD-QUADRANT OPERATION OF THE INTERSIL IRF130 SHOWS AGREEMENT BETWEEN THE PREDICTED VALUES OF THE ENHANCED SPICE II MODEL AND ACTUAL MEASURED VALUED OF DRAIN CURRENT vs DRAIN VOLTAGE AT DIFFERENT VALUED OF CONSTANT GATE VOLTAGE.



(a) (b)

FIGURE 11. THESE PLOTS OF DRAIN AND GATE VOLTAGES vs. TIME FOR CONSTANT GATE CURRENT SHOW AGREEMENT BETWEEN THE PREDICTIONS OF THE ENHANCED SPICE II MODEL (a) AND MEASURED PERFORMANCE OF THE INTERSIL IRF130 POWER M0SFET (b).

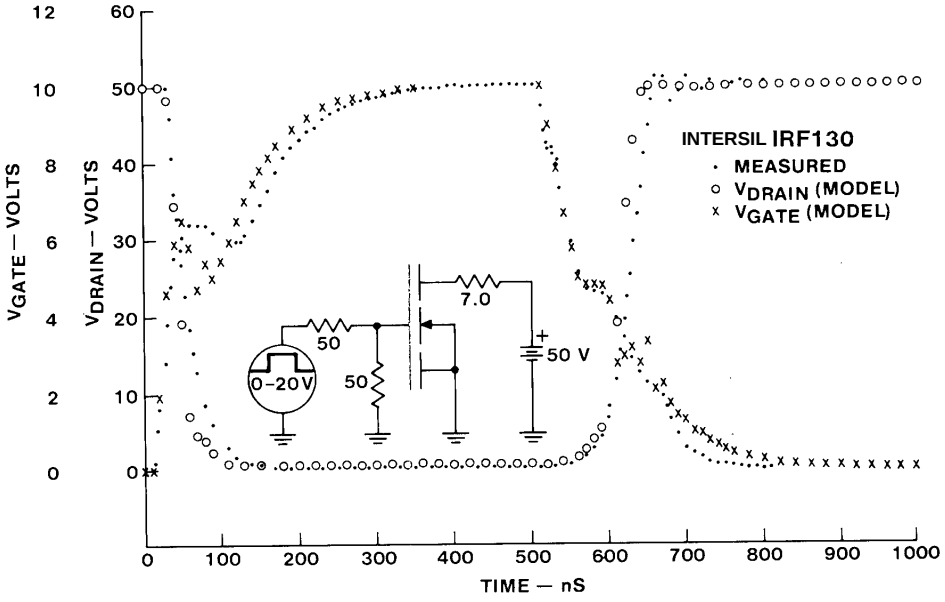


FIGURE 12. SWITCHING PERFORMANCE OF THE INTERSIL IRF130 POWER MOSFET IS CLOSELY PREDICTED BY THE ENHANCED SPICE II MODEL IN THIS PLOT OF MEASURED AND CALCULATED VALUES OF DRAIN AND GATE VOLTAGES vs. TIME IN A STANDARD SWITCHING CIRCUIT.

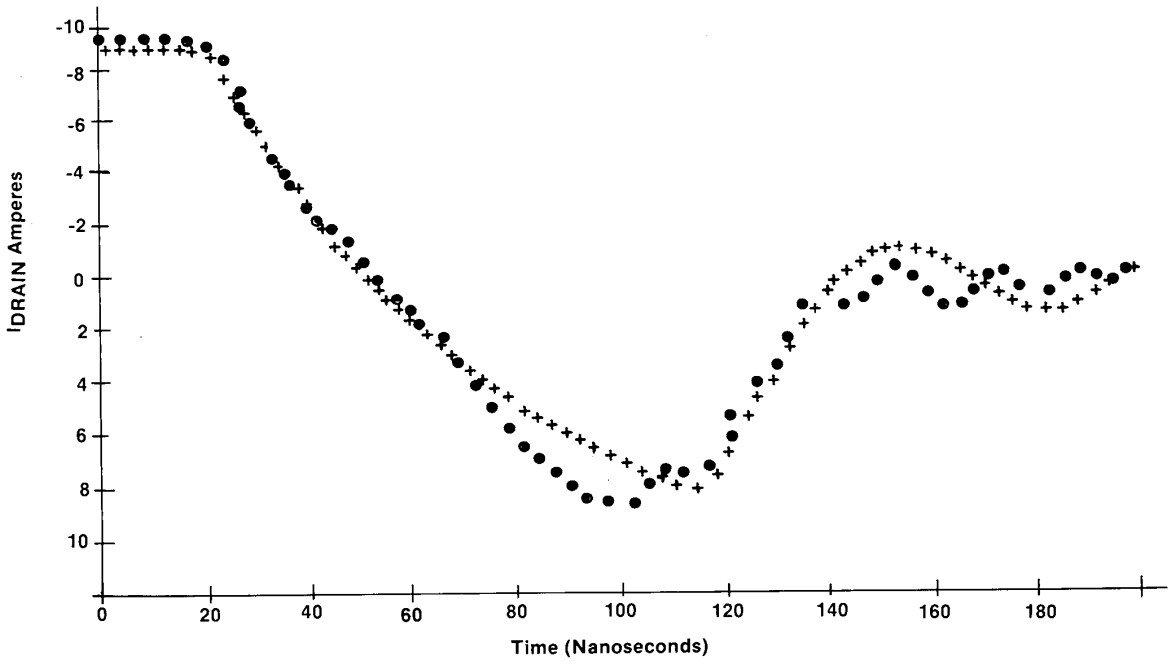


FIGURE 13. THE CALCULATED THIRD-QUADRANT DIODE RECOVERY WAVEFORM OF THE ENHANCE SPICE II MODEL SHOWS GOOD AGREEMENT WITH THAT ACTUALLY MEASURED FOR THE INTERSIL IRF130 POWER MOSFET

Finally, the enhanced model was used to compare calculated and measured body diode (D_{BODY} in Figure 2) recovery time curves in third-quadrant operation of the Intersil power MOSFET. Figure 13 shows the good agreement between predicted and actual results.

This approach provides excellent results when there is a need to model the performance of a power MOSFET. Not only will the approach update SPICE II (or other circuit simulation CAD program) so that it will simulate the latest state-of-the-art in MOS power, but it will allow quick analysis of every static and dynamic characteristic for suitability in a proposed design.

References

1. Wheatley, Jr., C.F. and Ronan Jr., H.R., "Switching Waveforms of the L^2FET: A 5-Volt Gate Drive Power MOSFET," Power Electronic Specialist Conference Record, June 1984, p. 238.

2. Ronan Jr., H.R. and Wheatley Jr., C.F., "Power MOSFET Switching Waveforms: A New Insight," Proceedings of Powercon 11, April 1984, p. C3.

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