## 1.3 Pulse-Width-Modulated Step-Up Converter/Regulator

The circuit of Fig. 1–4 can only produce a voltage lower than the input voltage. A switching mode converter capable of yielding a voltage higher than the input is shown in Fig. 1–6.

An inductor L1 and switch S1 are bridged across the input voltage source $V_{in}$. The switch S1 is operated at a high rate, anywhere from 3 to 50 kHz, and is closed for a time $T_c$ and open for time $T_o$ of the period $T_c + T_o$ $(= T)$. With the diode D1, filter capacity $C_o$, and load $R_L$ placed across the switch as shown, the output voltage is stepped up to the value

$$V_o = V_{in}(T_c + T_o)/T_o = V_{in}(1 + T_c/T_o)$$
$$= V_{in}/(1 - T_c/T)$$

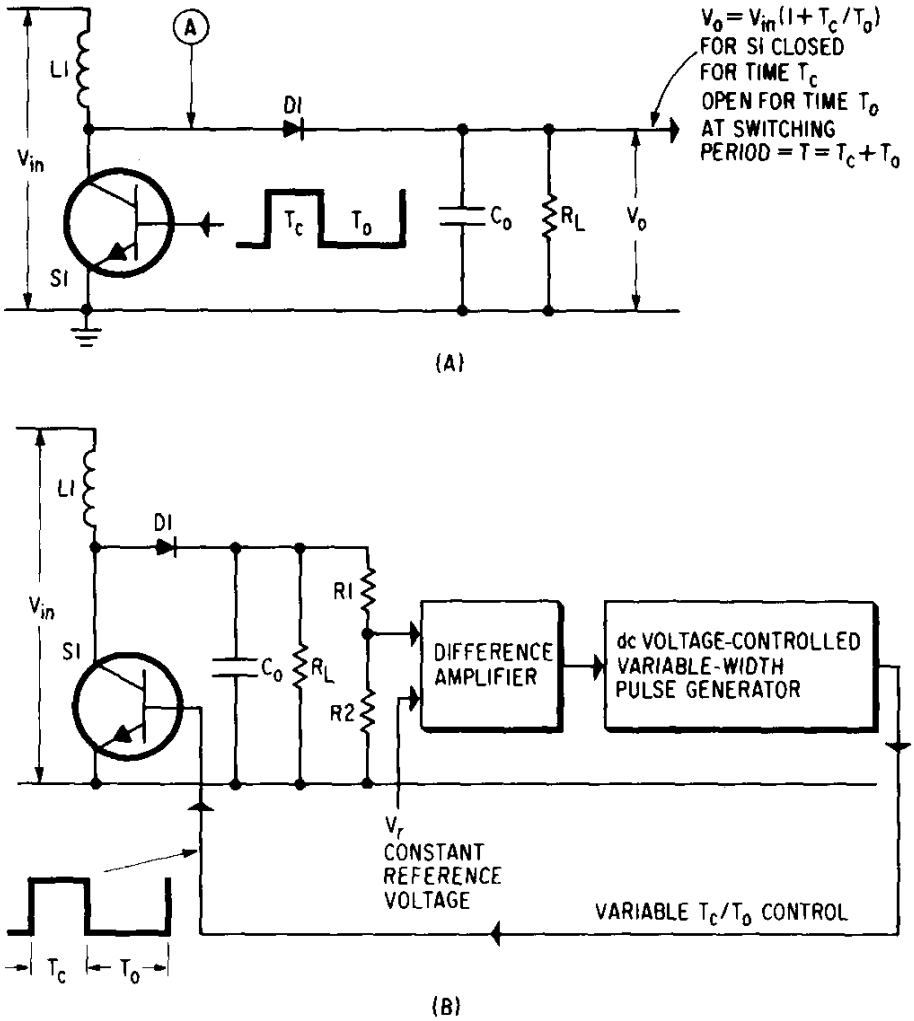


**Fig. 1–6.** (A) A shunt-switch voltage step-up converter. (B) Addition of a feedback loop to build a step-up switching regulator.

(as derived in Sect. 1.3.2). This circuit is often referred to as a "ringing choke" converter.

When S1 is closed, energy flows from the input source and is stored in L1. During this time, diode D1 is reverse biased, capacity $C_o$ supplies all the output current, and its stored energy $(C_oV_o^2)/2$ is somewhat depleted. When S1 opens, since current in an inductor cannot change instantaneously, an inductive voltage step appears across L1, making the bottom end of L1 positive relative to its top end. Diode D1 becomes forward biased, and the current initially flowing through L1 and S1 now continues flowing via diode D1 into the output capacitor $C_o$ and to the load.

The energy stored in L1 when S1 was closed, $(LI_{peak}^2)/2$, is transferred, when S1 is open, into the load and into the output capacitor to restore the energy it lost when S1 was closed and $C_o$ alone was driving the load. The magnitude of the inductive voltage step across L1 when S1 opens is controlled by the ratio of $T_c/T_o$. The larger the value of $T_c$, the greater is the peak current and energy stored in L1; hence, the higher must be the inductive voltage impulse across L1 during the time $T_o$ if the energy accumulated during $T_c$ is to be transferred out during $T_o$.

Like the series switching converter of Fig. 1–4, this too acts like a transformer without requiring a magnetic core. Assuming lossless switching, the circuit takes an input voltage $V_{in}$ at a dc current $I_{in}$ and steps it up to a higher voltage $V_{in}(T_c+T_o)/T_o$ at a lower output current $I_o=I_{in}T_o/(T_c+T_o)$.

### 1.3.1 Pulse-Width-Modulated Step-Up Converter Efficiency

The circuit (Fig. 1–6) is not truly lossless. In practical circuits, S1 is a saturated transistor with a 1-V drop for a time $T_c$; D1 is a silicon diode with a 1-V drop during $T_o$. The average value of input current flows through S1 for $T_c$, then through D1 for $T_o$. Thus, internal losses are $I_{in}(1)$ and efficiency is

$$E=\frac{P_o}{P_{in}}=\frac{V_oI_o}{V_oI_o+I_{in}(1)}$$

Since $I_{in}=I_o(T_c+T_o)/T_o$,

$$E=\frac{V_oI_o}{V_oI_o+\dfrac{I_o(T_c+T_o)(1)}{T_o}}$$

$$=\frac{V_o}{V_o+\dfrac{(T_c+T_o)(1)}{T_o}}=\frac{V_{in}}{V_{in}+1} \qquad (1\text{–}3)$$

This is the step-up converter efficiency considering only dc losses in the switch. And as discussed in Sect. 1.2.1, when ac voltage–current overlap losses are included, efficiency is approximately

$$E=\frac{V_{in}}{V_{in}+2} \qquad (1\text{–}3A)$$

This is the maximum possible efficiency. Low-level loss of the width control circuitry will lower this somewhat, but such step-up converter efficiencies of up to 95% are easily achievable.

### 1.3.2 Input–Output Voltage Relationship

The relationship of the output voltage to the $T_c/T_o$ ratio can be determined as follows. In the steady state, after a number of cycles, the output voltage stabilizes to the desired constant value $V_o$. Output ripple can be made as low as desired by proper choice of $C_o$. For a permissible ripple of $\Delta V_o$ and a dc output current of $I_o$, since the entire load must be supplied from $C_o$ for a time $T_c$, the value selected for $C_o$ must be $C_o = I_o T_c/\Delta V_o$.

Now when S1 is closed, there is a constant voltage $V_{in}$ across L1, and current in it rises linearly at a rate $\Delta I/\Delta T = V_{in}/\text{L1}$. Then the increment of current in L1 when S1 is closed for a time $T_c$ is

$$\Delta I\,(+) = (V_{in}/\text{L1})T_c$$

And when S1 is open, assuming the inductive kick has driven the bottom end of L1 up to the desired output $V_o$, the voltage across L1 is $V_o - V_{in}$. Now with the bottom end of L1 positive, current in L1 decreases at a rate $\Delta I/\Delta T = (V_o - V_{in})/\text{L1}$. Since S1 remains open for a time $T_o$, the decrease in L1 current in that interval is

$$\Delta I\,(-) = \frac{(V_o - V_{in})T_o}{\text{L1}}$$

But in the steady state, for each cycle, the current increase in L1 during $T_c$ must equal the decrease during $T_o$. Or

$$\Delta I\,(+) = \Delta I\,(-)$$

$$\frac{V_{in}T_c}{\text{L1}} = \frac{(V_o - V_{in})T_o}{\text{L1}}$$

Or

$$V_o = V_{in}\left(\frac{T_o + T_c}{T_o}\right)$$

$$= V_{in}(1 + T_c/T_o) \qquad (1\text{–}4)$$

Thus, by changing the ratio $T_c/T_o$, any desired step up can be obtained. Note, of course, that the switch S1, which is actually a transistor, is subjected to $V_o$ during $T_o$ and must have a voltage rating capable of taking that voltage with an adequate safety margin.

### 1.3.3 Pulse-Width-Modulated Shunt-Switch Step-Up Regulator

The step-up converter becomes a voltage regulator by the addition of a voltage sampling resistor chain, a constant voltage reference, difference amplifier, and a dc voltage-controlled variable-width pulse generator as shown in Fig. 1–6B.

As the input voltage varies, the ratio $T_c/T_o$ is automatically adjusted to maintain a constant output voltage. An increase in $V_{in}$ results in a decrease in $T_c/T_o$; a decrease in $V_{in}$ causes an increase in $T_c/T_o$ in accordance with Eq. 1–4.

This can be understood in a physical sense by considering an increase in $V_{in}$ for a fixed $T_c + T_o$. Since current in the inductor rises at a rate $dI/dT = V_{in}/\text{L}$, at larger $V_{in}$, more energy would be stored in L1 if $T_c$ remained fixed. Then if the increased stored energy had to be dissipated in the same $T_o$, output voltage would have to rise. Thus, the only way to keep the output constant is to decrease the energy stored by L1 during $T_c$ by decreasing the duration of $T_c$.

The circuit can be operated in a number of ways. The frequency or period can be kept constant and the ratio $T_c/T_o$ varied. Or often, $T_c$, the "on" time is kept constant and the operating frequency or period $T_c + T_o$ is adjusted to vary the ratio $T_c/T_o$. In either case, $V_o = V_{in}(1 + T_c/T_o)$.

Generally, a fixed frequency is preferred; as in many systems there usually is a fixed clock frequency, and it is desired to keep any noise voltages caused by such high-power switching locked in phase to the clock frequency. Yet, the circuit is often used in a constant $T_c$, variable period $(T_c + T_o)$ mode because of the availability of inexpensive integrated circuit control circuitry building blocks, such as voltage-controlled oscillators and fixed-width pulse generators.

The regulator also regulates against changes in load current. Because of the output impedance, a change—say, an output current increase—would tend to lower the output voltage. This is interpreted by the voltage sampling chain exactly as a change resulting from a line input change. The negative-feedback network thus changes the ratio $T_c/T_o$ to keep the output constant.

## 9.5 Width-Modulated Step-Up Switching Converters

This regulator is discussed in broad outline in Sect. 1.3, and its basic circuit diagram is shown in Fig. 1–6.

The regulator finds application, of course, wherever a higher voltage is required and the only source available is a lower-voltage one. There is no dc isolation from the negative terminal of the input source; hence, if the stepped-up output is to be used external to the power supply, the negative terminal of the input source must already be dc isolated from the ac line.

The step-up regulator finds its most frequent application as a step-up preregulator operating directly off the rectified ac line. Most often, such an ac line preregulator is a series-switch step-down regulator as described throughout this chapter (Fig. 9–1). But one undesirable aspect of the step-down preregulator is that it draws large amplitude and fast rise and fall time current steps from the input source (see Fig. 9–2C).

These chopped current steps are troublesome. Drawn through inductance of the wiring to the input source, they cause inductive voltage and current spikes that cross talk into other sensitive wires in the system. Even if local rfi filtering is used, the wiring from the series switch itself to the rfi filter can cause cross-talk problems. These chopped current pulses also impose a difficult ripple current rating on the rfi filter capacitor.

In contrast, the current drawn from the input source in the step-up switching regulator does not come in steps with sharp rise and fall times. Rather, it is a dc current that never drops to zero but has a slow triangular ripple component superimposed on it (Fig. 9–33D). This gives far less rfi and internal cross-talk problems and is one of the chief advantages of the step-up regulator.

A detailed description of step-up regulator current and voltage waveforms will clarify its operation and simplify making the various design decisions.

### 9.5.1 Critical Waveforms in Step-Up Switching Converters

The major elements of the converter and its critical waveforms are shown in Fig. 9–33. The major design decisions are selection of the output capacitor output inductor L and switch transistor Q. Since the inductor carries a dc component, it must be designed so as not to saturate at maximum load current. Also, maximum voltage to which the transistor switch is subjected must be calculated to verify that it operates within its ratings.

The basic operation of the converter is considered in Sect. 1.3. There it is pointed out that when Q1 is on (Fig. 9–33), diode D1 is reverse biased and $C_o$ must supply the full output load current by itself. The switch is closed for a time $T_c$ and is open for a time $T_o$. Output voltage is (from Eq. 1–4): $V_o = V_{in}\ (1 + T_c/T_o)$.

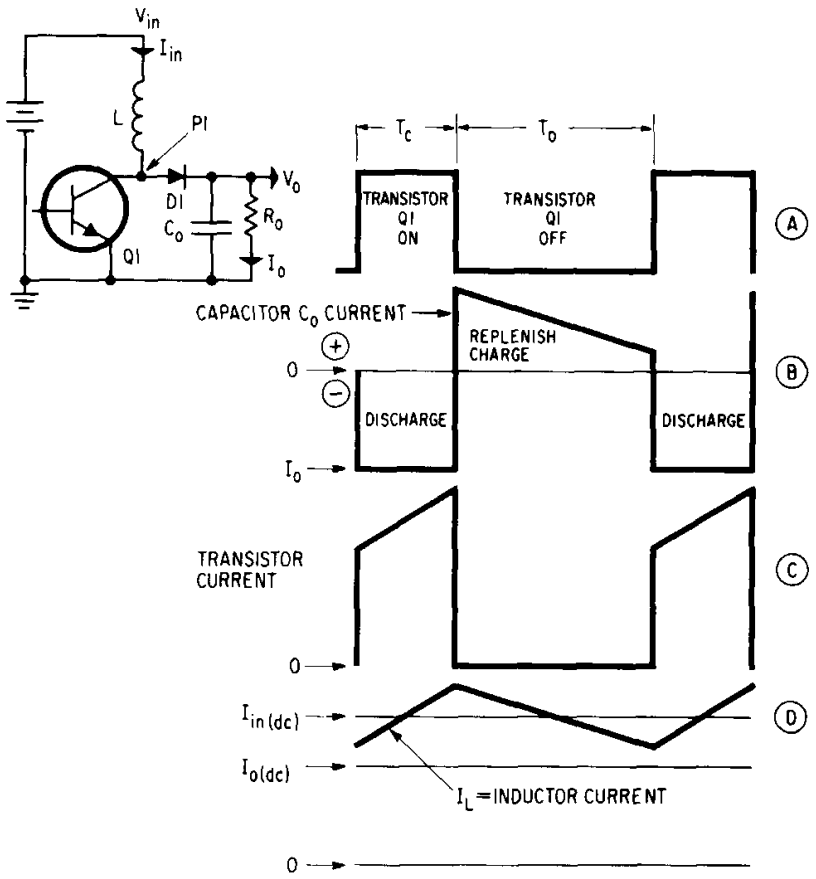


**Fig. 9–33.** Critical waveforms in step-up switching regulator for $T_c/T_o = 0.5$; $V_o = 1.5\ V_{in}$; and $I_{in} \cong 1.5\ I_o$.

### 9.5.2 Selection of Output Filter Capacitor

Now if $C_o$ must supply the full load current for a time $T_c$ and if its voltage droop at the end of $T_c$ is to be no more than $\Delta V_o$, $C_o$ is given by $C_o = I_o(T_c/\Delta V_o)$.

But $T_o + T_c = T = 1/f$, where $T$ is the switching period and $f$ is its frequency. Then

$$T_c = T - T_b$$

but $$V_o = [(T_c + T_o)/T_o]V_{in} = (T/T_o)V_{in}$$

and $$T_c = T - T_o = T - (V_{in}/V_o)T = T[(V_o - V_{in})/V_o];$$

then $$C_o = I_o T_c/\Delta V_o = I_o(V_o - V_{in})/fV_o\Delta V_o \qquad (9\text{–}27)$$

This fixes the value of $C_o$ for a desired output voltage $V_o$, minimum ripple $\Delta V_o$, switching frequency $f$, output voltage and current $V_o$ and $I_o$, and nominal input voltage $V_{in}$.

### 9.5.3 Selection of Energy Storage Inductor

Figure 9–33 shows current supplied by $C_o$ during $T_c$ to be $-I_o$ (current out of the top of $C_o$ is taken to be negative). Now, during $T_o$, Q1 opens and the inductive kick at the bottom end of L drives point P1 positive until diode D1 connects. Now L supplies load current to $R_o$ at a voltage $V_o$ and must also supply

current to replenish the charge $C_o$ lost when it alone was feeding the load. The charge $C_o$ lost during $T_c$ is $I_o T_c/C$. Thus, during $T_o$, the volt second area of the current flowing into $C_o$ must equal $I_o T_c$ or

$$\int_o^{T_o} I_c dt = I_o T_c$$

The actual current flowing into $C_o$ during $T_o$ is the difference between the load current and the inductor current.

But the inductor current has a dc or average value plus a ramp component. This average is determined as follows: Assuming no internal losses for the moment, $V_{in} I_{in} = V_o I_o$. Now, $I_{in}$ is the average current taken from $V_{in}$ or the average current flowing into the inductor $I_L$. Since $V_o = V_{in}\,(1 + T_c/T_o)$ (from Eq. 1-4),

$$I_{in(dc)} = I_o \left(\frac{V_o}{V_{in}}\right) = \frac{I_o V_{in}\,(1 + T_c/T_o)}{V_{in}} = I_o \left(\frac{T_c + T_o}{T_o}\right)$$

The ripple component of current is a ramp, for during $T_c$ there is a constant voltage of $V_{in}$ across L and after a time $T_c$ current increases in it by an amount $+\Delta I_L = V_{in} T_c/L$. When Q1 is open for a time $T_o$, the voltage across L reverses polarity and the current in it ramps down by $-\Delta I_L = (V_o - V_{in})/L$. And in the steady state $+\Delta I_L$ during $T_c$ is equal to $-\Delta I_L$ during $T_o$.

The magnitude of $\Delta I_L$ is selected just as in the series-switch inductor (Sect. 9.1.5, Eq. 9-14) so that the peak inductor current ($=I_{in(dc)} + \Delta I_L/2$) is no more than 20% greater than the maximum average dc current. This makes it easier to keep the inductor from saturating. It also minimizes the peak current in Q1 and reduces dissipation and stress in it. It also makes lower in value the minimum load at which it is possible to operate. The current in the inductor at the bottom of the ripple triangle in Fig. 9-30 must not be permitted to fall to zero before the end of $T_o$.

Hence, $\Delta I_L$ is chosen as 1.4 $I_{in(dc,\,nom)}$ and the inductor is calculated from:

$$\mathrm{L} = \frac{V_{in(nom)} T_c}{\Delta I_L} = \frac{V_{in(nom)} T_c}{1.4 I_{in(dc,\,nom)}}$$

But, from above, $T_c = (V_o - V_{in})/f V_o$. And assuming negligible losses,

$$V_o I_o = V_{in(nom)} I_{in(dc,\,nom)}$$

or

$$I_{in(dc,\,nom)} = V_o I_o / V_{in(nom)}$$

Then

$$\mathrm{L} = \frac{V_{in(nom)} T_c}{1.4 I_{in(dc,\,nom)}} = \frac{(V_{in(nom)})^2 (V_o - V_{in(nom)})}{1.4 f V_o^2 I_o} \qquad (9\text{-}28)$$

This gives the required value in terms of output voltages, current, nominal input voltage, and switching frequency – all of which are known.

The current in $C_o$ during $T_o$ can now be seen in Fig. 9-33B. It is the difference between the output load current $I_o$ and the inductor current during $T_o$. That last current is the sum of the dc input current plus the downward-going ramp $-\Delta I_L$ calculated above. It can be seen that the volt second area of the current waveform into $C_o$ during $T_o$ is equal to the volt second area of the current taken out of $C_o$ during $T_c$.

### 9.5.4 Transistor Voltage and Current and Power Stresses

The maximum voltage stress on transistor Q1 is, of course, $V_o$, which is an input design parameter and is $V_{in}(1 + T_c/T_o)$. Thus, unlike dc/dc converter circuits, the transistor can be stressed to more than twice the dc input.

The current step in the transistor Q1 can be approximated for power dissipation purposes by a square step of amplitude $I_p = I_o(V_o/V_{in})$. This lasts for a time $T_c$ and the resultant dc dissipation in the transistor is $I_o(V_o/V_{in})(V_{ce(sat)})(T_c/T)$. To a close approximation, it can be assumed the high-voltage–high-current overlap losses during turnon and turnoff (Sect. 2.1.3) will equal these losses.

### 9.5.5 Avoiding Switching Inductor Saturation

The inductor carries a dc current $I_o(V_o/V_{in})$ and has a peak-to-peak ripple component of 40% of that value (Sect. 9.1.4). The inductor should be designed to avoid saturation either by use of a gapped core or a powdered iron core as discussed in Sect. 9.1.8.

### 9.5.6 Width-Modulated, Step-Up Regulator

All that is required to make a step-up regulator out of the converter is the same set of elements shown in Fig. 9–1 for the step-down regulator. These are a negative-feedback loop consisting of an output voltage sampling resistor chain, a difference amplifier, and triangle voltage level to pulse width converter to control the switch duty cycle. These have all been discussed in connection with the step-down regulator and need not be considered here.

The width modulator, which is the heart of the feedback chain, can be the same triangle-level comparator. Often, if fixed frequency operation is not necessary, the closed-switch time is kept constant and the period varied by the voltage at the output of the main dc error amplifier. This is currently best done with a number of available integrated dircuit voltage-controlled oscillators that generate a fixed pulse width at a frequency determined by a dc input control voltage.

## 9.6 Integrated-Circuit Building Blocks for Control Circuitry in Pulse-Width-Modulated dc/dc Converters

Integrated circuit modules such as binary counters, multiple NAND gates in one package, and timers that can be used either as monostable multivibrators ("one shots") or astable multivibrators (square-wave oscillators) offer a simple and inexpensive way to implement pulse-width control circuitry. At the time of this writing such building blocks can be bought for less than 50 cents (100 + quantity). All the circuitry required to generate the usual two 180° out-of-phase variable-width drive pulses can be assembled from three to five integrated circuit building blocks, three resistors, and two capacitors. In the usual case, the width-modulated output pulses must control bases of power transistors whose emitters are referenced to input ground. This, in off-the-ac-line rectifiers, may be 150–300 V away from output ground, which is the reference for the variable-width control pulses. Thus, to provide the dc isolation between the generator of the variable-width pulses and the power inverter bases, two additional low-power transistors and two pulse transformers may be required.

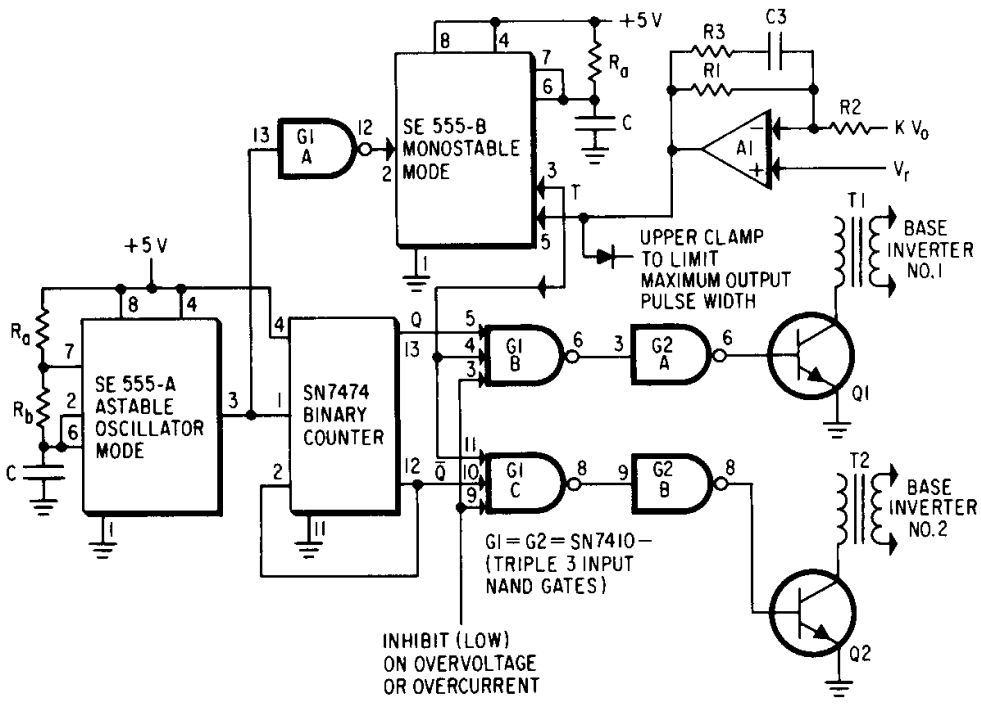


**Fig. 9–34.** Pulse-width control circuitry using integrated-circuit building blocks.

A large variety of logic configurations and building blocks may be used to generate the two 180° out-of-phase width-modulated control signals. Generally, the scheme is to route a variable-width pulse alternately through two NAND gates on alternate half cycles under control of a binary counter, which is triggered at the leading edge of the variable-width pulse. A typical example of such a logic configuration is shown in Fig. 9–34.

Figure 9–34 makes use of two triple three-input NAND gate modules (SN 7410) and a dual D type flip-flop (SN7474 of which only one is used) operated as a binary counter by connecting its $\overline{Q}$ output to its data input and two SE555[8] timers. The SE555 is a useful timer in that it can be operated as a free-running square-wave oscillator (astable mode) and also as a monostable multivibrator ("one shot").

As a one shot, the SE555 emits a positive-going output pulse at its output (pin 3) when triggered by a negative-going pulse at the "trigger input" (pin 2). The duration of the positive output pulse (with control pin 5 connected to ground via a capacitor) is given by $T_o = 1.1R_aC$. The pulse-width sensitivity to supply voltage variation is 0.02%/volt, to temperature variation (assuming constant $R_a$ and $C$) is 0.01%/°C. The output pulse width may be controlled by varying the dc voltage at the "control" input (pin 5). Variation of this voltage from 0.2 to $0.6V_{cc}$ varies the pulse width from $0.22R_aC$ to $1.1R_aC$. Since the dc output voltage of the converter is proportional to the "on" time pulse width, output voltage may be kept constant by driving pin 5 of the "one shot" by an error voltage that is proportional to the difference between a reference voltage and a fraction of the output dc voltage.

[8] Signetics Co. Data Sheet.

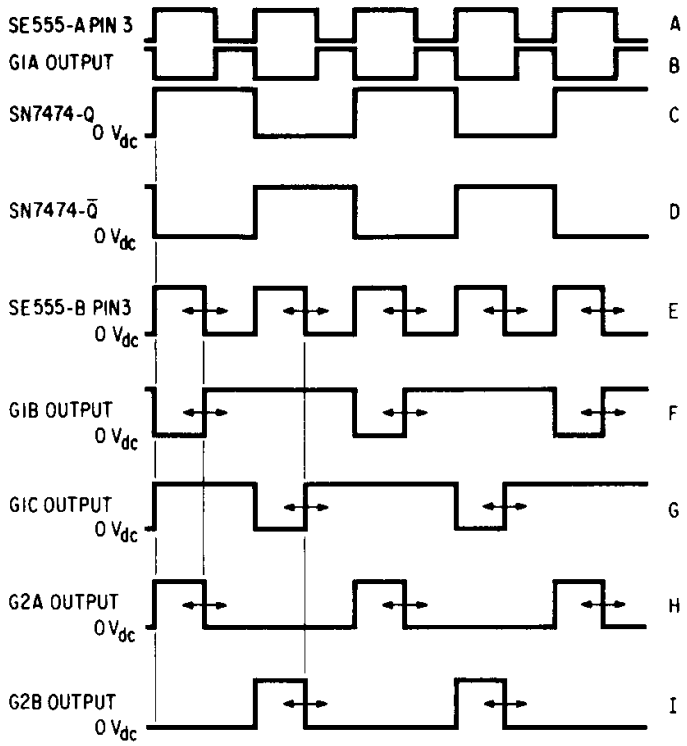


**Fig. 9–35.** Waveforms for Fig. 9–34.

The SE555 can also be used as a free-running square-wave oscillator if connected as shown in Fig. 9–34(SE555A). In this mode, the duration of the positive portion of the square wave at pin 3 is given by $T_p = 0.685(R_a + R_b)C$; the duration of the negative portion by $T_n = 0.685R_bC$. The period of the square-wave oscillator is then

$$T = T_p + T_n = 0.685(R_a + 2R_bC)$$

and its frequency is

$$f = \frac{1}{T} = \frac{1.46}{R_a + 2R_bC}$$

The operation of the logic block diagram of Fig. 9–34 can be understood from the waveforms in Fig. 9–35.

Figure 9–35A shows the output at SE555A, pin 3. Frequency of this astable multivibrator is chosen to be twice the desired square-wave frequency of the converter. Relative duration of the positive and negative portions of the waveform are not important. The SN7474 connected as shown operates as a binary counter and changes state at every positive-going transition of the "clock" signal at pin 1. Out-of-phase outputs from the binary counter are shown as Q, $\overline{Q}$ in Figs. 9–35C and 9–35 D.

Monostable SE555B requires a negative-going transistor at trigger pin 2 to generate its output pulse. The third NAND gate of G1 (G1A) is used as a single input inverter to generate the negative-going transition (Fig. 9–35B) at each change of state of the binary counter.

G1A also serves the valuable purpose of providing a slight delay in the leading edge of the SE555B positive-going output signal beyond the binary

counter output voltage transition. This prevents false narrow negative-going output spikes from positive NAND gates G1B and G1C. Such false narrow outputs occur if there is a momentary overlap of high voltage as one input falls while the other input rises. Such false narrow output pulses can destroy the power inverters by causing false turnons, increasing their power dissipation or causing simultaneous inverter conduction.

Postive logic NAND gates G1B and G1C serve to route the pulse from SE555B through to their respective outputs on alternate half cycles as negative-going pulses (Figs. 9–35C and 9–35F). NAND gates G2A and G2B are used as single-input inverters to give positive-going output pulses on alternate half cycles (Figs. 9–35H and 9–35I). Transistors Q1 and Q2 are pulse amplifiers and the pulse transformers T1 and T2 permit delivering the output pulses to the power inverter bases at any arbitrary dc level.

The negative-feedback loop is closed through error amplifier A1—an operational amplifier whose dc gain is R1/R2. Its gain phase shift-versus-frequency characteristic is tailored by R3 and C3. As the output voltage tends to rise, $KV_o$ moves upward and A1 output moves downward. Now the lower voltage at SE555B pin 5 reduces its output pulse width and also that of the positive-going pulses at the outputs of G2A and G2B. This reduces the power-inverter-on times and decreases the dc output voltage of the filter in the secondary of the main power transformer.

An upper clamp is provided at pin 5 to limit the maximum output pulse width to less than about 90% of the half period of the binary counter output.

The logic of Fig. 9–34 is a general illustration of what can be done. It can be simplified in various ways. Gate G1A may be eliminated by narrowing the negative portion of the SE555A output and using the negative transition to trigger SE555B, the positive-going transition (perhaps 1 to 2 $\mu$sec later) to drive the binary counter. This permits using a single Quad-2 (four two-input NAND gates in one package) for what is now in two packages (G1B, C, G2A, B). The 555 timers are presently available as two timers in one package (556). The package count is thus now down to three (not counting error amplifier A1) as compared to five in Fig. 9–34.

Just recently, integrated circuit modules that perform all of the functions of Fig. 9–34 in one single package have become available.[9] Although presently they are more expensive, the decreased package count may make them more economical when assembly and logistic costs are considered.

### 9.6.1 Motorola MC3420 Switching-Regulator Control Circuit Module[10]

The usual switching-regulator control circuit consists of two variable-width rectangular pulses which occur symmetrically within alternate half cycles of the fundamental switching frequency and are capable of being width modulated by the dc control voltage. This dc control voltage is the amplified difference between the voltage to be regulated and a reference voltage.

The circuit in Fig. 9–35 generates such pulses using four to five conventional integrated circuits (timers, NAND gates), each in its own dual-in-line

[9] Motorola MC 3420, Silicon General SC1524.

[10] Data and information courtesy of Motorola, Inc.

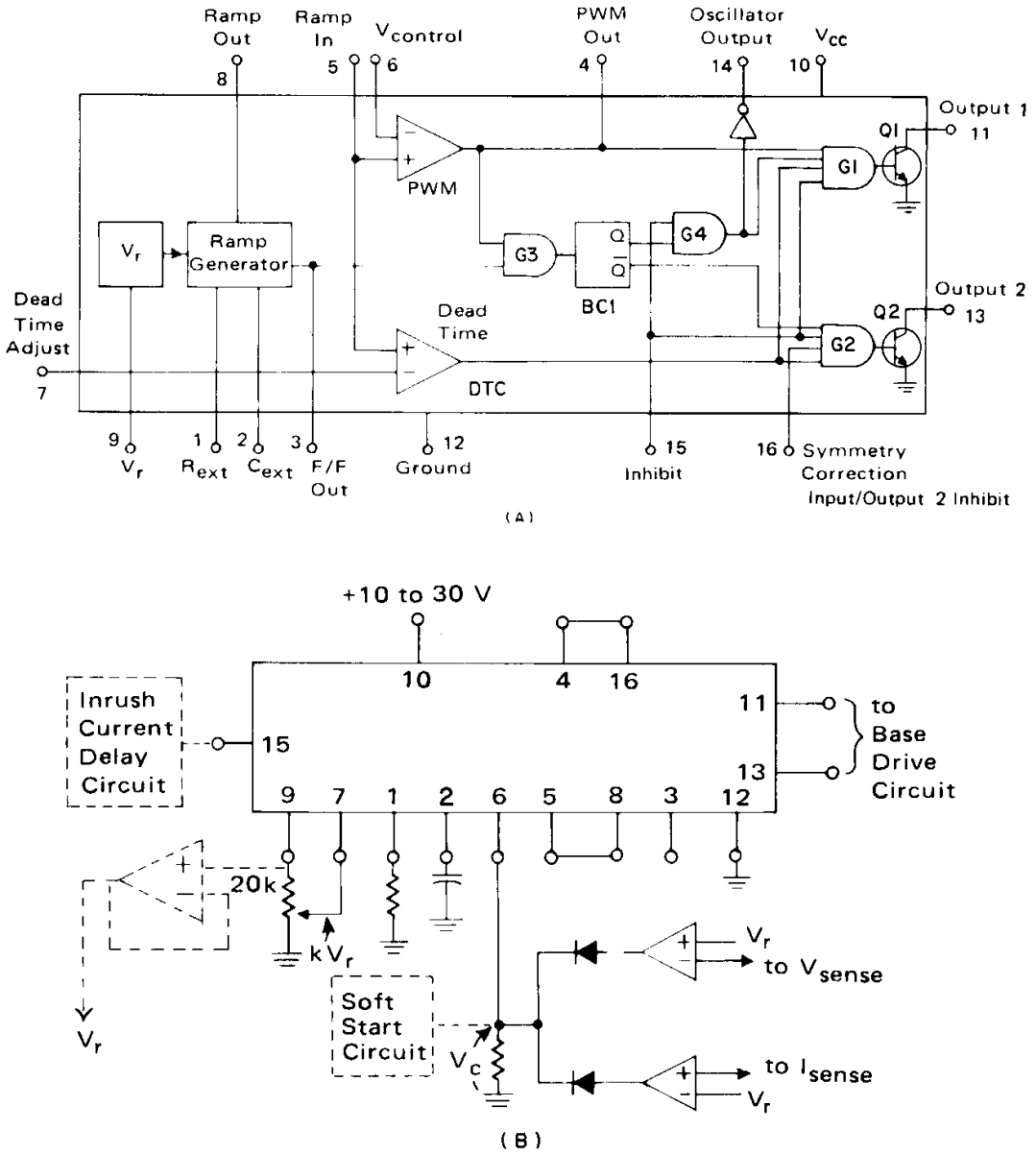


**Fig. 9–36.** Motorola MC3420 IC switching regulator control circuit. (A) Block diagram. (B) Typical application. (*Courtesy* Motorola, Inc.)

(DIP) package. The Motorola MC3420 (Fig. 9–36) performs all and somewhat more of the functions of the circuit in Fig. 9–35 in a single integrated circuit in one DIP package. Complete details can be obtained from the manufacturer's data sheet, but briefly its operation is as follows:

The ramp generator in Fig. 9–36A contains a flip-flop. When the circuit is connected as in Fig. 9–36B, the "ramp generator" is a free-running triangle oscillator whose frequency is fixed by the values of the external resistor ($R_{ext}$) and external capacitor ($C_{ext}$), as shown in Fig. 9–36D. Because of internal circuit details, when the flip-flop signal at pin 3 is high, the triangle ramps downward; when the flip-flop signal at pin 3 is low, the triangle ramps upward. The triangle ramps between +2 and +6 V.

The triangle is compared (pin 8 connected to pin 5) against a dc voltage level in triangle comparator PWM. Whenever the triangle voltage at pin 5 is

voltages of −5 to +30 V, the step-down turns ratio is high, and the impedance reflected into the secondary is low In most cases, collector saturation resistances reflected into secondaries can be kept down to 0.005–0.01 ohm.

The diode rectifier impedance, $R_d$, is a function of the diode current capacity and operating point on its $V_c$–$I_c$ curve. This can be seen in the curves of Fig. 2–4 for some high-speed rectifier diodes of various current ranges. These diodes are obtainable with reverse voltage ratings from 50 to 600 V. Their impedance ranges from 0.1 ohm at the 1-A current level to 0.01 ohm at the 20- to 30-A points.

Thus, by proper choice of transistors and rectifier diodes, total output impedance ($R_d + R_{ts}$) seen looking back into a secondary can be kept in the range of 0.01–0.10 ohm. Then, in a converter such as in Fig. 2–1, operating with constant or preregulated dc input voltage, load-current changes of 5 A centered about 20 A will cause output voltage changes of only about 0.05 V.

This is often a constant enough voltage, and hence, by preregulating the dc input to a converter and choosing high-current, low-impedance rectifying diodes for each secondary, further regulation after the secondaries is unnecessary.

### 2.1.7 High-Frequency Operation

Almost the first decision to be made in designing a square-wave converter is the choice of operating frequency. When such converters first came into widespread use, operating frequencies of 5–10 kHz were generally chosen. But higher frequencies, up to 20–50 kHz, have distinct advantages. The two largest elements in the converter—the power transformer and output filter capacitor—become much smaller at higher frequencies. It will be shown in Chap. 8 that the maximum available load power from a given transformer is proportional to its operating frequency. Thus, for a given load power, doubling the operating frequency will roughly halve the volume of the transformer.

In Sect. 2.1.4 it was pointed out that the size of the output filter capacity depends on the rise and fall times of collector voltage waveforms. The higher-frequency transistors used with higher-frequency converters have faster output rise and fall times. Voltage notches at the secondary are thus narrower and require smaller capacitors for the same filtering.

There is a further nonelectrical advantage in going to frequencies above 10 kHz. Despite the most elaborate precautions, converters operating below 10 kHz will generate an audible hum that generally can be heard at a distance of 10–20 ft. For equipment with operators in the vicinity for long periods of time, e.g., in a computer room, this is a distracting and an absolutely prohibitive drawback. Operating frequency should be above about 18 kHz to avoid the audible hum problem.

Currently, new designs are being done at 20–50 kHz. This is now possible because of the current availability of high-current, high-voltage transistors having low turn-on, turn-off, and storage times. Thus, there are presently available transistors with a maximum current rating of 10 A and a voltage rating of

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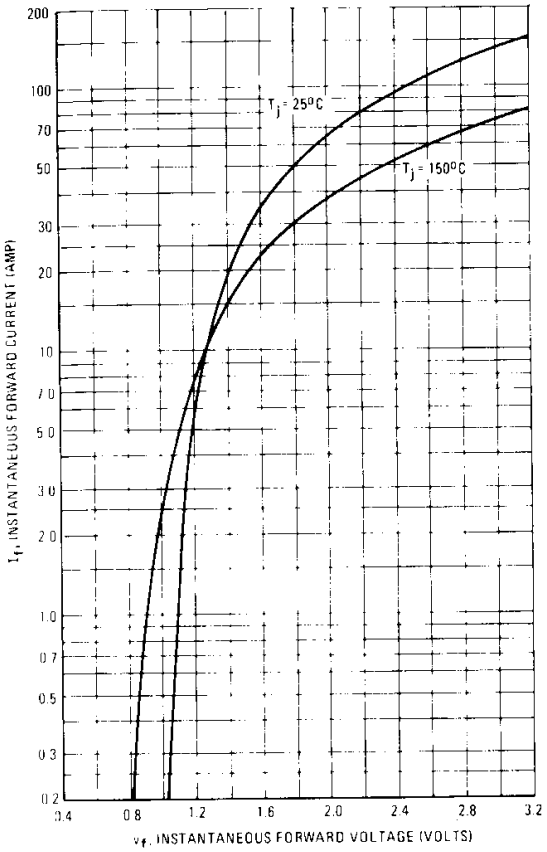
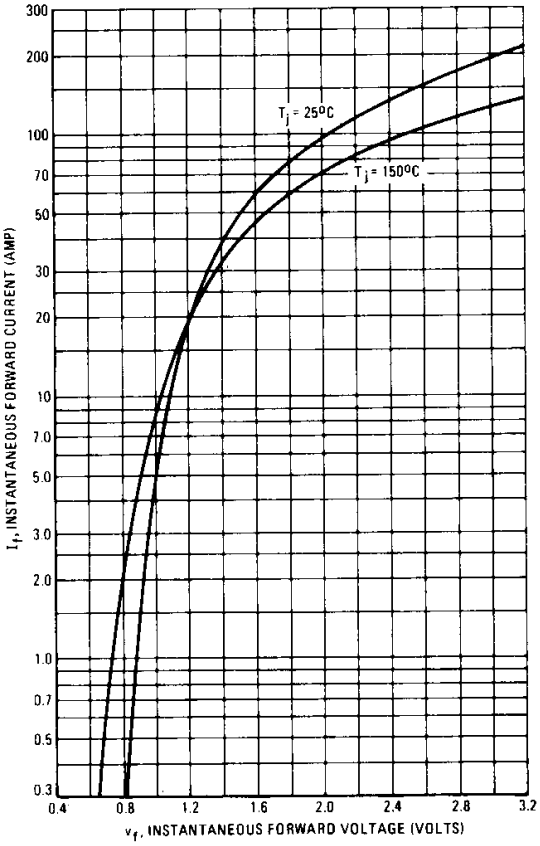
**Fig. 2–4.** Fast-switching rectifier diodes with low output impedance. (A) 1N3879 series, 6-A diodes. (B) 1N3889 series, 12-A diodes. (C) 1N3899 series, 20-A diodes. (D) 1N3909 series, 30-A diodes. (*Courtesy* Motorola, Inc.)

FORWARD VOLTAGE



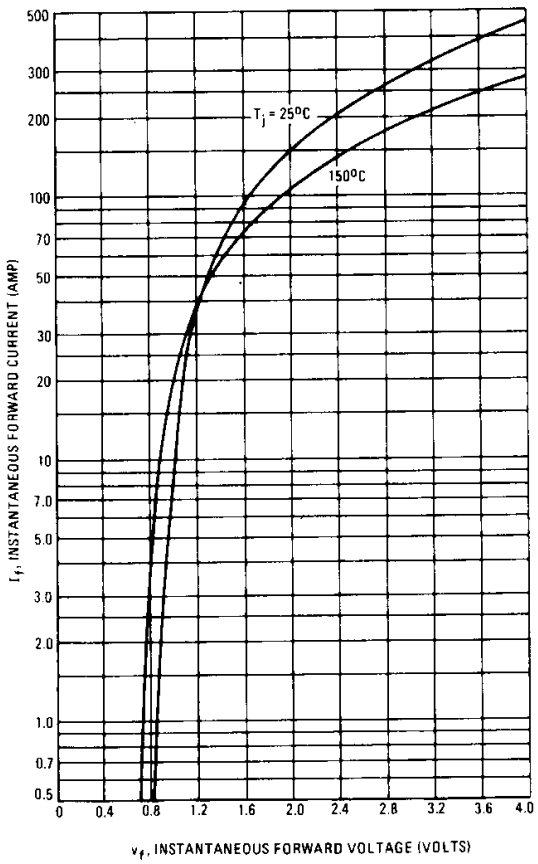

(A)

FORWARD VOLTAGE



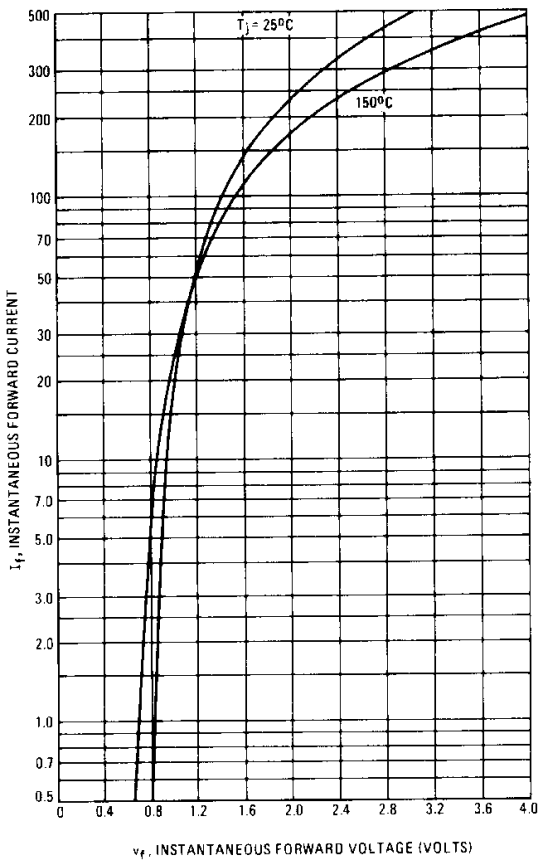

(B)

FORWARD VOLTAGE




(C)

FORWARD VOLTAGE




(D)

400 V. By operating at high forward and reverse input (forward and reverse input currents one-tenth the output current), turn-on and turn-off times can be kept down to 0.5 $\mu$sec each. Storage times can be kept down to 1 $\mu$sec by high reverse input drive by circuit tricks preventing transistor saturation.

As discussed in Sect. 2.1.3, there will be an overlap of high voltage and current during these relatively slow turn-on, turn-off, and storage times. To keep efficiency high, this "overlap" dissipation must last for as small a fraction of a half cycle as possible. Generally, the sum of rise, fall, and storage times should be permitted to be no more than 10% of the half periods. Thus, $T/2 = 10(t_r + t_f + t_s)$ or $T = 20(t_r + t_f + t_s)$. And for the abovementioned transistors, whose sum of rise, fall, and storage times is 2 $\mu$sec, the maximum frequency at which reasonably good efficiency is possible is

$$f = \frac{1}{T} = \frac{1}{20(2 \times 10^{-6})} = 25 \text{ kHz}$$

At 50 kHz, with the same high-voltage–high-current overlap, the duty cycle of the spike of "overlap" dissipation is higher, and the average internal dissipation is greater. If the thermal design is good enough, transistors whose sum of rise, fall, and storage times is 2 $\mu$sec can be used up to 50 kHz if the reduced efficiency is acceptable—but 50 kHz is about an upper limit. Higher-frequency operation is possible for low-power converters in which low efficiency is no serious drawback.